

**PROTECTION PRODUCTS**
**Description**

RailClamps are surge rated diode arrays designed to protect high speed data interfaces. The SR series has been specifically designed to protect sensitive components which are connected to data and transmission lines from overvoltage caused by electrostatic discharge (**ESD**), electrical fast transients (**EFT**), and **lightning**.

The unique design of the SR series devices incorporates four surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

The low capacitance array configuration allows the user to protect two high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges.

**Features**

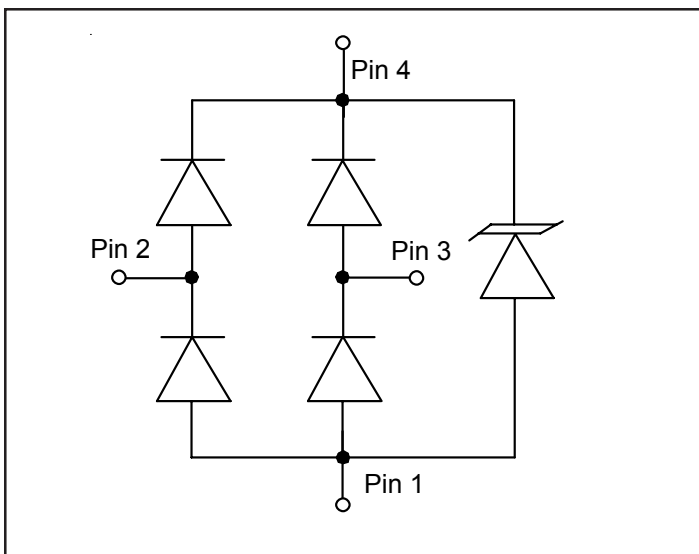
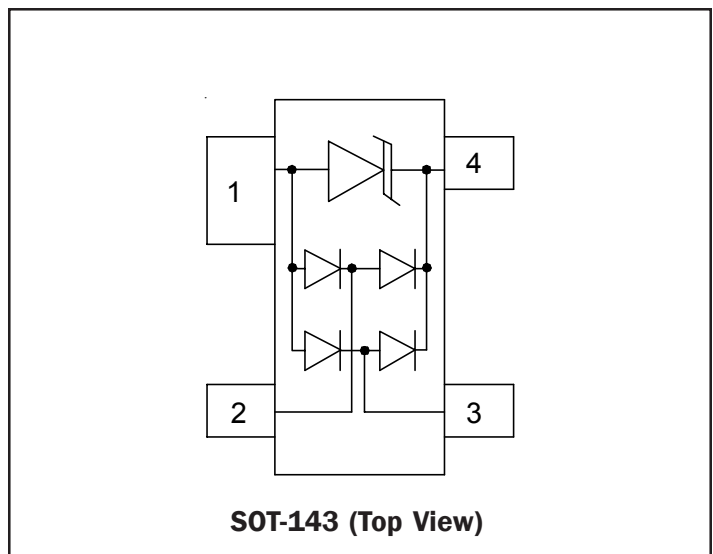
- ◆ ESD protection to  
**IEC 61000-4-2 (ESD) ±15kV (air), ±8kV (contact)**  
**IEC 61000-4-4 (EFT) 40A (5/50ns)**  
**IEC 61000-4-5 (Lightning) 24A (8/20µs)**
- ◆ Array of surge rated diodes with internal TVS Diode
- ◆ Protects two I/O lines
- ◆ Low capacitance (<10pF) for high-speed interfaces
- ◆ Low clamping voltage
- ◆ Low operating voltage: 5.0V
- ◆ Solid-state silicon-avalanche technology

**Mechanical Characteristics**

- ◆ JEDEC SOT-143 package
- ◆ UL 497B listed
- ◆ Molding compound flammability rating: UL 94V-0
- ◆ Marking : R05
- ◆ Packaging : Tape and Reel per EIA 481

**Applications**

- ◆ USB Power & Data Line Protection
- ◆ Ethernet 10BaseT
- ◆ I<sup>2</sup>C Bus Protection
- ◆ Video Line Protection
- ◆ T1/E1 secondary IC Side Protection
- ◆ Portable Electronics
- ◆ Microcontroller Input Protection
- ◆ WAN/LAN Equipment
- ◆ ISDN S/T Interface

**Circuit Diagram**

**Schematic & PIN Configuration**


**PROTECTION PRODUCTS**
**Absolute Maximum Rating**

| Rating   | Symbol    | Value         | Units |
|--|-----------|---------------|-------|
| Peak Pulse Power (tp = 8/20μs)                 | $P_{pk}$  | 500           | Watts |
| Peak Pulse Current (tp = 8/20μs)               | $I_{pp}$  | 25            | A     |
| Peak Forward Voltage ( $I_f = 1A$ , tp=8/20μs) | $V_{FP}$  | 1.5           | V     |
| Lead Soldering Temperature                     | $T_L$     | 260 (10 sec.) | °C    |
| Operating Temperature                          | $T_J$     | -55 to +125   | °C    |
| Storage Temperature                            | $T_{STG}$ | -55 to +150   | °C    |

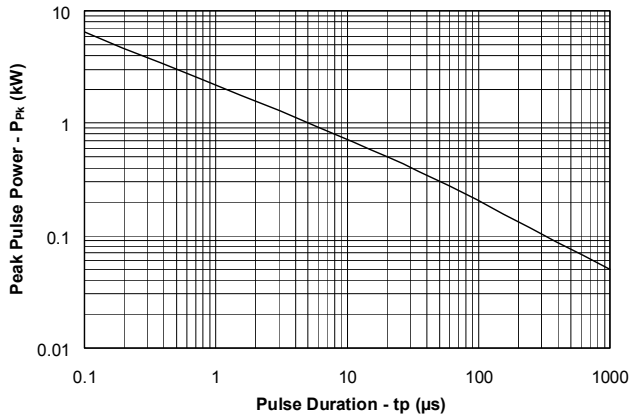
**Electrical Characteristics**

| SR05                      |           |   |         |         |         |       |
|---------------------------|-----------|---|---------|---------|---------|-------|
| Parameter                 | Symbol    | Conditions  | Minimum | Typical | Maximum | Units |
| Reverse Stand-Off Voltage | $V_{RWM}$ |   |         |         | 5       | V     |
| Reverse Breakdown Voltage | $V_{BR}$  | $I_t = 1mA$   | 6       |         |         | V     |
| Reverse Leakage Current   | $I_R$     | $V_{RWM} = 5V, T=25°C$                              |         |         | 5       | μA    |
| Clamping Voltage          | $V_C$     | $I_{pp} = 1A, tp = 8/20μs$                          |         |         | 9.8     | V     |
| Clamping Voltage          | $V_C$     | $I_{pp} = 10A, tp = 8/20μs$                         |         |         | 12      | V     |
| Clamping Voltage          | $V_C$     | $I_{pp} = 25A, tp = 8/20μs$                         |         |         | 20      | V     |
| Junction Capacitance      | $C_J$     | Between I/O pins and Ground<br>$V_R = 0V, f = 1MHz$ |         | 6       | 10      | pF    |
|                           |           | Between I/O pins<br>$V_R = 0V, f = 1MHz$            |         | 3       |         | pF    |

PROTECTION PRODUCTS

Typical Characteristics

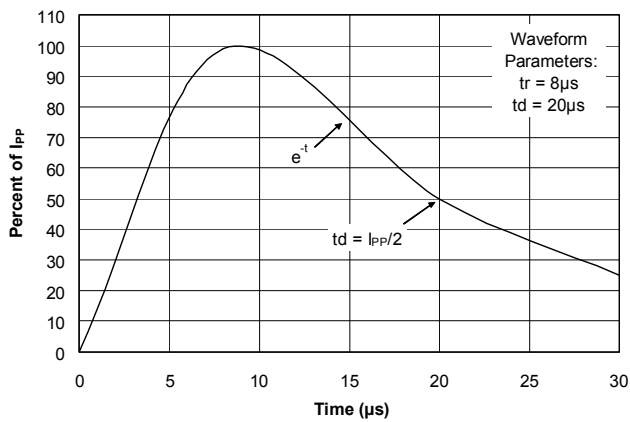
Non-Repetitive Peak Pulse Power vs. Pulse Time



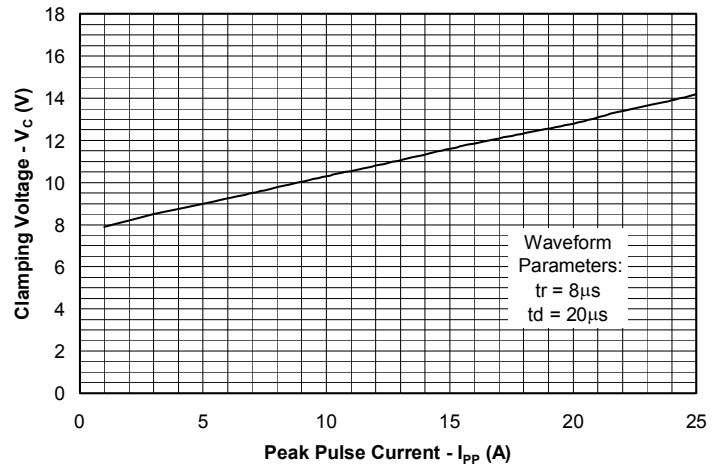
Power Derating Curve



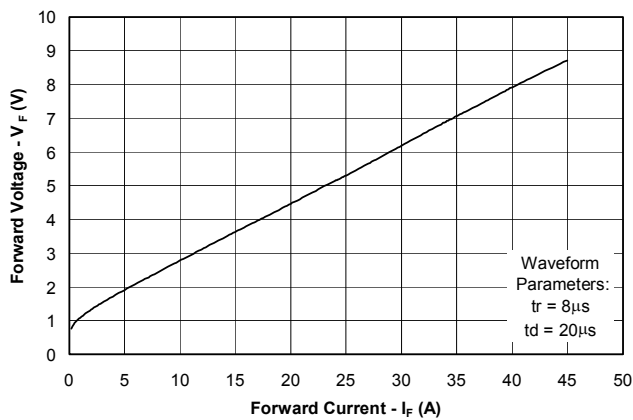
Pulse Waveform



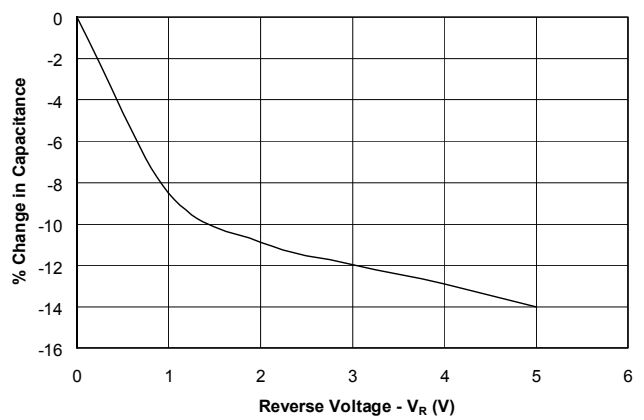
Clamping Voltage vs. Peak Pulse Current



Forward Voltage vs. Forward Current



Capacitance vs. Reverse Voltage



**PROTECTION PRODUCTS**

**Applications Information**

**Device Connection Options for Protection of Two High-Speed Data Lines**

The SR05 TVS is designed to protect two data lines from transient over-voltages by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage (plus diode  $V_F$ ) the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at pins 2 and 3. The negative reference (REF1) is connected at pin 1. This pin should be connected directly to a ground plane on the board for best results. The path length is kept as short as possible to minimize parasitic inductance.

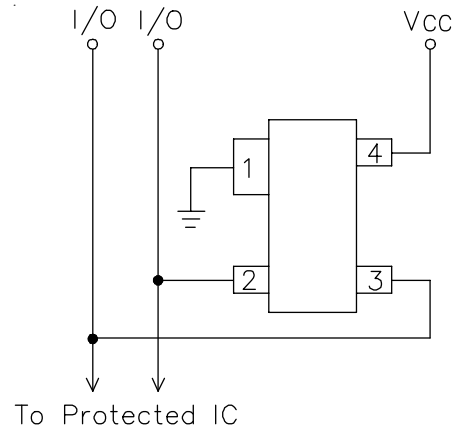
The positive reference (REF2) is connected at pin 4. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect pin 4 directly to the positive supply rail ( $V_{CC}$ ). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail.
2. The SR05 can be isolated from the power supply by adding a series resistor between pin 4 and  $V_{CC}$ . A value of  $10k\Omega$  is recommended. The internal TVS and steering diodes remain biased, providing the advantage of lower capacitance.
3. In applications where no positive supply reference is available, or complete supply isolation is desired, the internal TVS may be used as the reference. In this case, pin 4 is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).

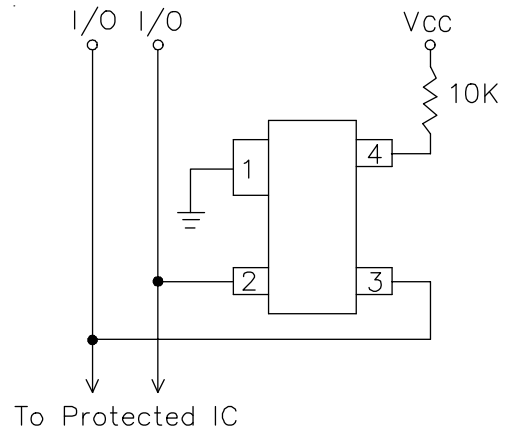
**ESD Protection With RailClamps**

RailClamps are optimized for ESD protection using the rail-to-rail topology. Along with good board layout, these devices virtually eliminate the disadvantages of using discrete components to implement this topology. Consider the situation shown in Figure 1 where discrete diodes or diode arrays are configured for rail-to-rail protection on a high speed line. During positive duration ESD events, the top diode will be forward biased when the voltage on the protected line exceeds the reference voltage plus the  $V_F$  drop of the diode.

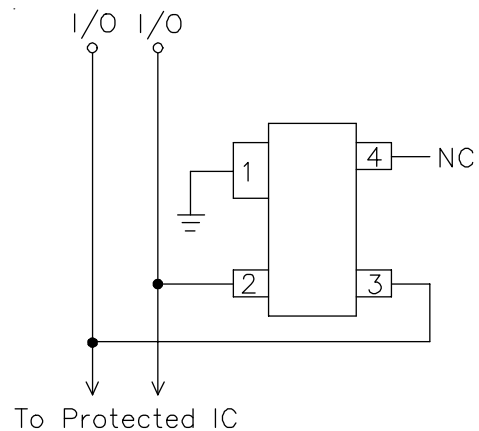
**Data Line and Power Supply Protection Using  $V_{CC}$  as reference**



**Data Line Protection with Bias and Power Supply Isolation Resistor**



**Data Line Protection Using Internal TVS Diode as Reference**



**PROTECTION PRODUCTS**

**Applications Information (continued)**

For negative events, the bottom diode will be biased when the voltage exceeds the  $V_F$  of the diode. At first approximation, the clamping voltage due to the characteristics of the protection diodes is given by:

$$V_C = V_{CC} + V_F \quad (\text{for positive duration pulses})$$

$$V_C = -V_F \quad (\text{for negative duration pulses})$$

However, for fast rise time transient events, the effects of parasitic inductance must also be considered as shown in Figure 2. Therefore, the actual clamping voltage seen by the protected circuit will be:

$$V_C = V_{CC} + V_F + L_P di_{ESD}/dt \quad (\text{for positive duration pulses})$$

$$V_C = -V_F - L_G di_{ESD}/dt \quad (\text{for negative duration pulses})$$

ESD current reaches a peak amplitude of 30A in 1ns for a level 4 ESD contact discharge per IEC 61000-4-2. Therefore, the voltage overshoot due to 1nH of series inductance is:

$$V = L_P di_{ESD}/dt = 1 \times 10^{-9} (30 / 1 \times 10^{-9}) = 30V$$

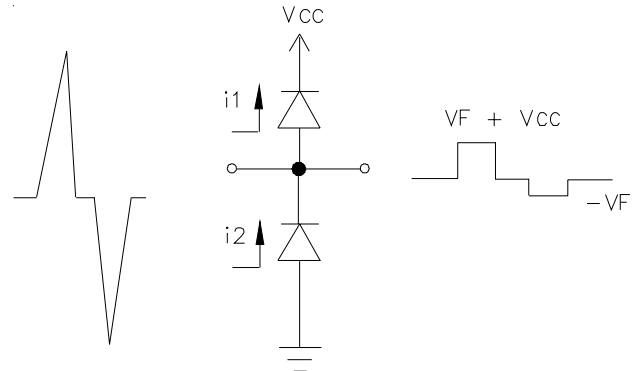
Example:

Consider a  $V_{CC} = 5V$ , a typical  $V_F$  of 30V (at 30A) for the steering diode and a series trace inductance of 10nH. The clamping voltage seen by the protected IC for a positive 8kV (30A) ESD pulse will be:

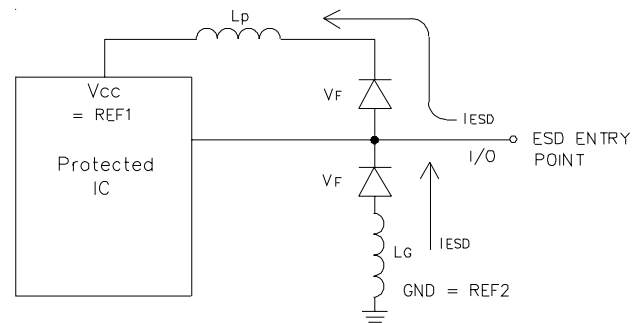
$$V_C = 5V + 30V + (10nH \times 30V/nH) = 335V$$

This does not take into account that the ESD current is directed into the supply rail, potentially damaging any components that are attached to that rail. Also note that it is not uncommon for the  $V_F$  of discrete diodes to exceed the damage threshold of the protected IC. This is due to the relatively small junction area of typical discrete components. It is also possible that the power dissipation capability of the discrete diode will be exceeded, thus destroying the device.

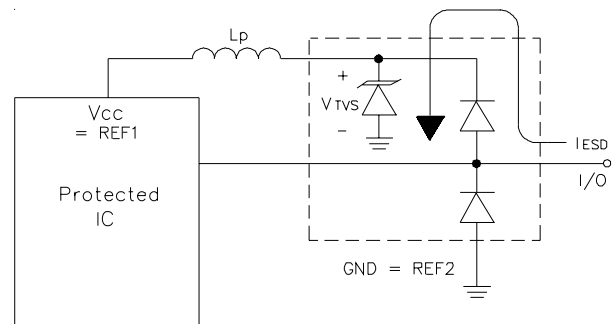
The RailClamp is designed to overcome the inherent disadvantages of using discrete signal diodes for ESD suppression. The RailClamp's integrated TVS diode helps to mitigate the effects of parasitic inductance in



**Figure 1 - "Rail-To-Rail" Protection Topology (First Approximation)**



**Figure 2 - The Effects of Parasitic Inductance When Using Discrete Components to Implement Rail-To-Rail Protection**



**Figure 3 - Rail-To-Rail Protection Using RailClamp TVS Arrays**

## PROTECTION PRODUCTS

### Applications Information (*continued*)

the power supply connection. During an ESD event, the current will be directed through the integrated TVS diode to ground. The total clamping voltage seen by the protected IC due to this path will be:

$$V_C = V_{F(\text{RailClamp})} + V_{\text{TVS}}$$

This is given in the data sheet as the rated clamping voltage of the device. For a SR05 the typical clamping voltage is <16V at  $I_{pp}=30A$ . The diodes internal to the RailClamp are low capacitance, fast switching devices that are rated to handle transient currents and maintain excellent forward voltage characteristics.

### Universal Serial Bus ESD Protection

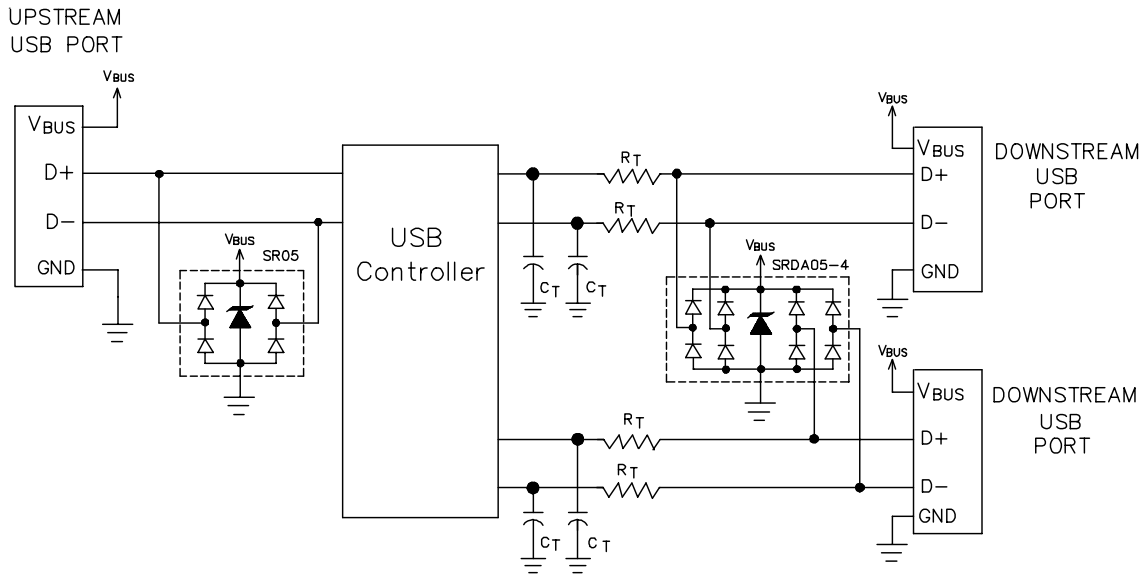
The figure below illustrates how to use the SR05 to protect one upstream USB port and the SRDA05-4 to protect two downstream USB ports. When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device. Reference Semtech application note SI96-18 for further information.

### Matte Tin Lead Finish

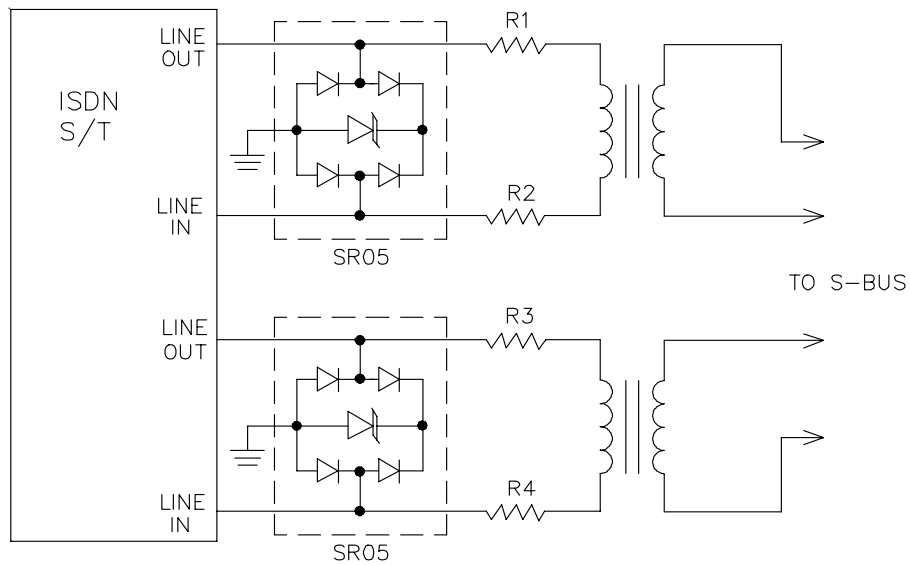
Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

PROTECTION PRODUCTS

Typical Applications



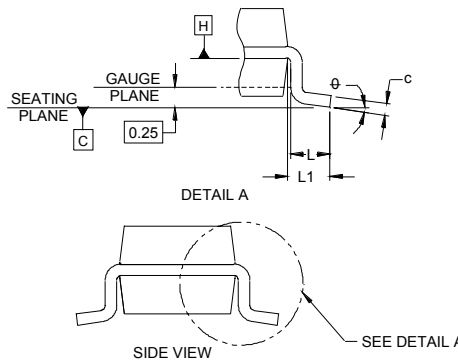
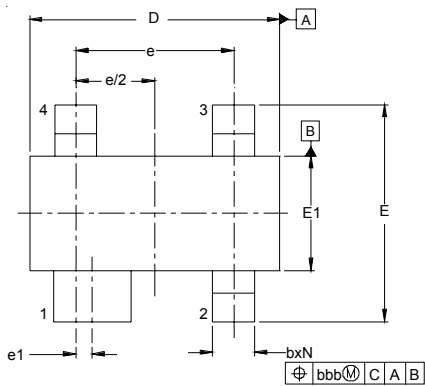
Universal Serial Bus ESD Protection



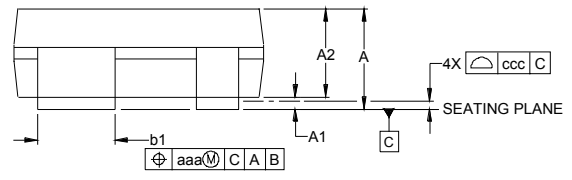
ISDN S/T Interface Protection

PROTECTION PRODUCTS

Outline Drawing - SOT-143

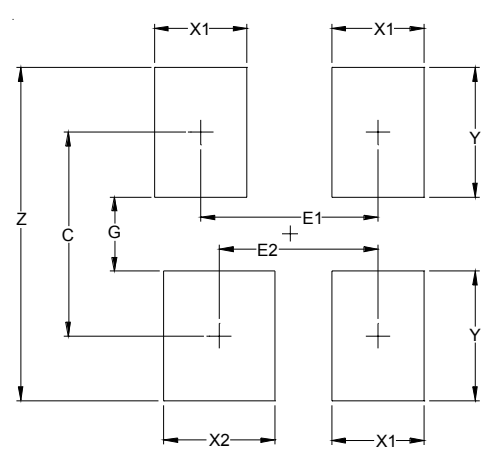


| DIM    | INCHES |        | MILLIMETERS |        |      |
|--------|--------|--------|-------------|--------|------|
|        | MIN    | NOM    | MIN         | NOM    |      |
| A      | .031   | -      | .048        | 0.80   | 1.22 |
| A1     | .000   | -      | .006        | 0.013  | 0.15 |
| A2     | .029   | .035   | .042        | 0.75   | 0.90 |
| b      | .011   | -      | .020        | 0.30   | 0.51 |
| b1     | .029   | -      | .037        | 0.76   | 0.94 |
| c      | .003   | -      | .008        | 0.08   | 0.20 |
| D      | .110   | .114   | .120        | 2.60   | 2.90 |
| E      | .082   | .093   | .104        | 2.10   | 2.37 |
| E1     | .047   | .051   | .055        | 1.20   | 1.30 |
| e      | .075   | -      | 1.92        | BSC    |      |
| e1     | .008   | -      | 0.20        | BSC    |      |
| L      | .015   | .020   | .024        | 0.40   | 0.50 |
| L1     |        | (.021) |             | (0.54) |      |
| N      | 4      | -      | 4           | -      |      |
| $\phi$ | 0°     | -      | 8°          | 0°     | 8°   |
| aaa    | .006   | -      | 0.15        | -      |      |
| bbb    | .008   | -      | 0.20        | -      |      |
| ccc    | .004   | -      | 0.10        | -      |      |



- NOTES:
1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
  2. DATUMS **-A-** AND **-B-** TO BE DETERMINED AT DATUM PLANE **-H-**
  3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
  4. REFERENCE JEDEC STD TO-253, VARIATION D.

Land Pattern - SOT-143



| DIMENSIONS |        |             |
|------------|--------|-------------|
| DIM        | INCHES | MILLIMETERS |
| C          | (.087) | (2.20)      |
| E1         | .076   | 1.92        |
| E2         | .068   | 1.72        |
| G          | .031   | 0.80        |
| X1         | .039   | 1.00        |
| X2         | .047   | 1.20        |
| Y          | .055   | 1.40        |
| Z          | .141   | 3.60        |

- NOTES:
1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
  2. REFERENCE IPC-SM-782A.



**PROTECTION PRODUCTS****Marking Codes**

| <b>Part Number</b> | <b>Marking Code</b> |
|--------------------|---------------------|
| SR05               | R05                 |

**Ordering Information**

| <b>Part Number</b> | <b>Lead Finish</b> | <b>Qty per Reel</b> | <b>Reel Size</b> |
|--------------------|--------------------|---------------------|------------------|
| SR05.TC            | SnPb               | 3,000               | 7 Inch           |
| SR05.TCT           | Pb free            | 3,000               | 7 Inch           |

**Contact Information**

Semtech Corporation  
Protection Products Division  
200 Flynn Road, Camarillo, CA 93012  
Phone: (805)498-2111 FAX (805)498-3804