FT838D/FT838R Application Design Guideline

Abstract

Features and application circuit for PSR controller FT838D/FT838R are presented in this guideline. Key performance, operation principle and typical solution design flow are also presented in this guideline.

Application

- Charger for Mobile Phone/PDA/Camera
- Adapter for ADSL & Cordless Telephone
- LED Lighting Product, such as Spotlight, LED Bulb etc.
- Best Replacement Solution for Linear Power Supply and RCC Discrete Power Supply

Features

- Eliminates Opto-coupler & Shunt Regulator 431
- PFM Mode for Enhanced Efficiency
- Frequency Dithering Technique eases EMI Design
- Cycle by Cycle Current Limit
- Over Voltage Protection
- Under Voltage Lock Out
- Short-circuit Protection
- Built-in Cable Voltage Drop Compensation
- Line Compensation for High Output Current Accuracy across Low & High Line Voltage

IC Version & Pin Configuration

Version	Cable Voltage Drop Compensation Rate
FT838D0	0%
FT838D1	3%
FT838D2	6%
FT838D3	9%
FT838R	N/A

Table 1. Version & Cable Voltage Drop Compensation for FT838D/FT838R

Output cable voltage drop compensation is built inside FT838D. User can select different version for actual output cable size and length. FT838R is tailored towards LED driver application, hence no cable compensation is needed.

Pin Order	Pin Name	I/O	Pin Description
1	FB	I	Output voltage sense pin
2	GND	I	Ground of the IC.
3	CS	I	Current sense pin.
4	OUT	O	Driving pin for external NPN base or MOS gate
5	VCC	I	Power supply for the IC.

Table 2：Pin Configuration and Function

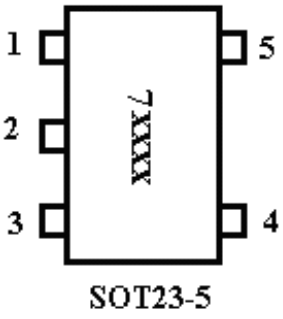


Figure 1. Pin Assignments

Typical Application Circuit

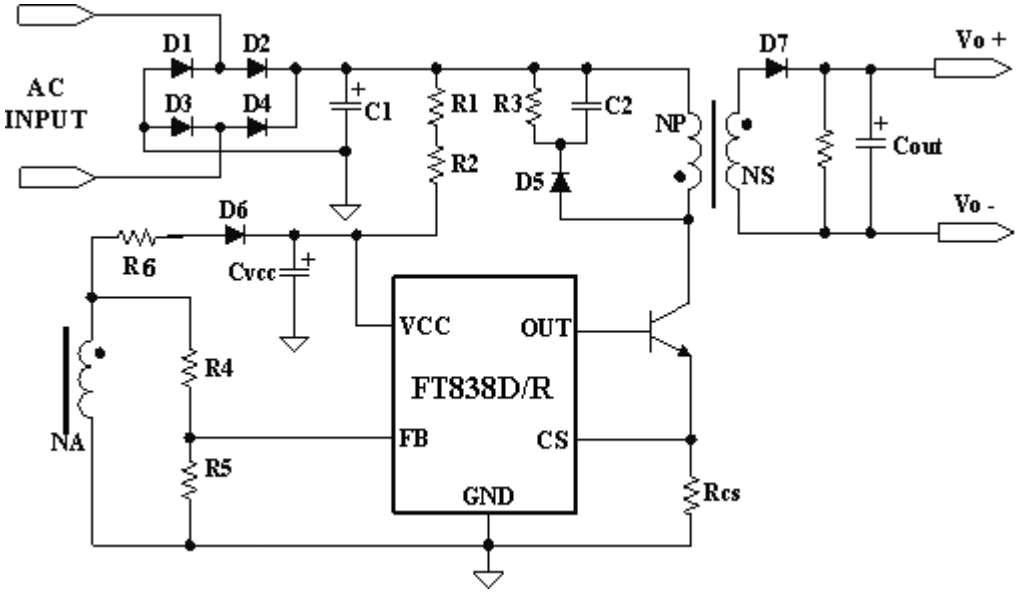


Figure 2. Typical Application Circuit Diagram

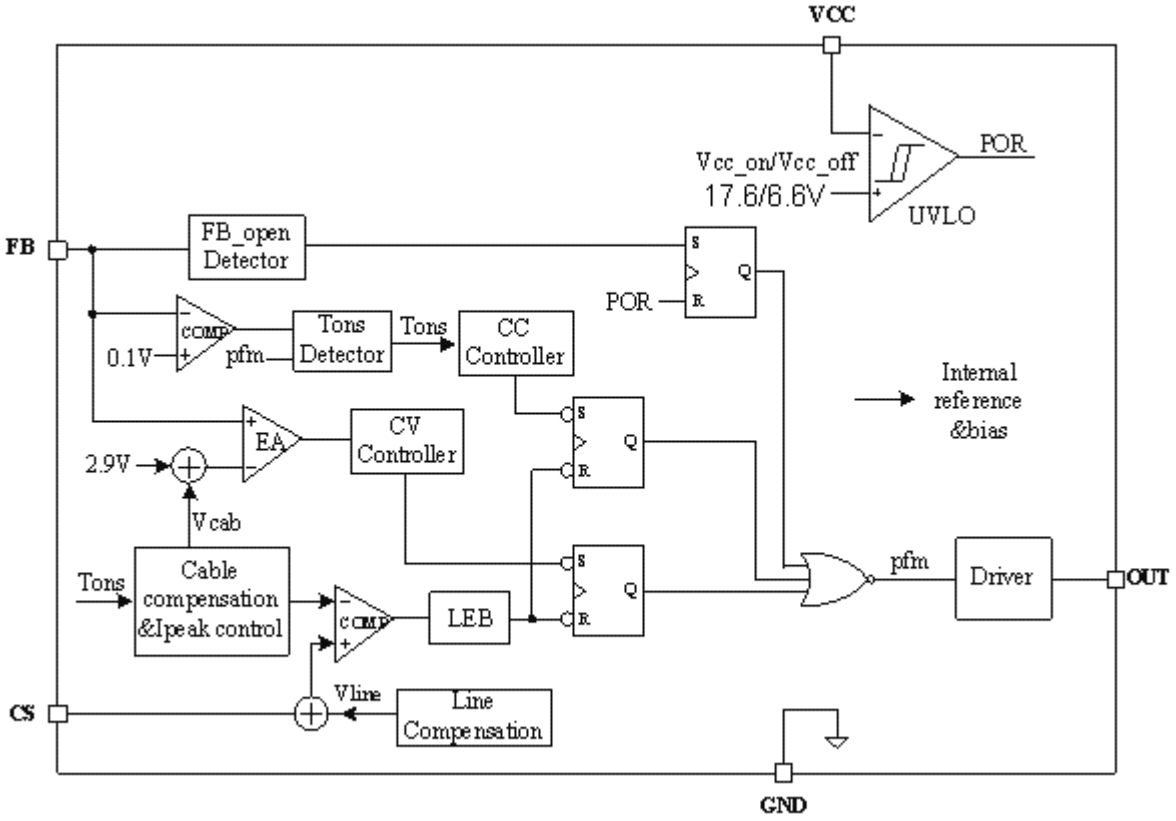


Figure 3. Block Diagram

Introduction

The FT838D/FT838R PSR controller IC integrates many features that effectively enhance the comprehensive performance of low power fly-back converters. The PSR topology simplifies system design and lowers system material cost. The system EMI design is made easy by the built-in frequency dithering, resulting in small volume and light weight system solutions.

The FT838D/FT838R works under Pulse Frequency Modulation (PFM) mode; operating frequency decreases with lighter output load, resulting in small power consumption at light loading condition. The maximum start-up current of FT838D is within 5uA, so startup resistor's value can be very large to lower the stand-by power consumption.

The FT838D/FT838R provides many protection functions. Under voltage lock out for AC input is easily realized via Pin FB. Cycle by cycle current limiting and constant current control ensure the over current protection (OCP) under heavy load. Moreover, in the event of primary side voltage feedback resistors short or open, the controller can shut down quickly; when the abnormal situation is removed, the system will re-start up automatically.

The FT838D/FT838R can realize constant voltage and constant current functions with very few external components.

Block Diagram

Constant Voltage Control

The PSR control method can realize precise constant voltage and constant current control without requiring the opto-coupler and shunt regulator 431 on secondary side. Figure 2 is the typical application circuit. Figure 3 shows the IC block diagram. Figure 4 lists a few key waveforms. The output status is sensed from the transformer auxiliary winding when power NPN/MOS switches off. The controller utilizes a unique sampling way to detect output voltage and discharge time of secondary winding. The sensed voltage on Pin FB is compared against a precision reference voltage Vfb. The error amplifier output is modulated to determine the switch-off time of NPN/MOS to realize the precise output voltage regulation.

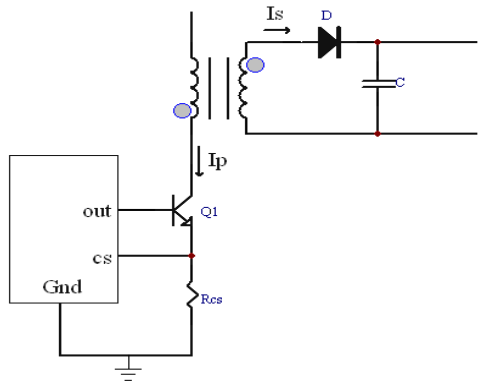
Constant Current Control

From figure 4，output current in flyback topology working under discontinuous conduction mode (DCM) can be obtained from Equation (1)

$$I_O = \frac{2 \times N_{ps} \times V_{csth}}{7 \times R_{cs}} \qquad (1)$$

where,
Nps is turn ratio between primary and secondary side
Rcs is current sensing resistor in primary side.
Vcsth is the voltage limit on current sensing resistor, which is internally set to 0.55V.

According to above equation (1), output current Io can be calculated with Nps and Rcs. With Nps and Rcs determined, the controller IC regulates the constant output current Io by adjusting the turn off time of NPN/MOS. The controller IC can realize precise and stable constant current output with good transformer designs. A design example is given at later chapters.



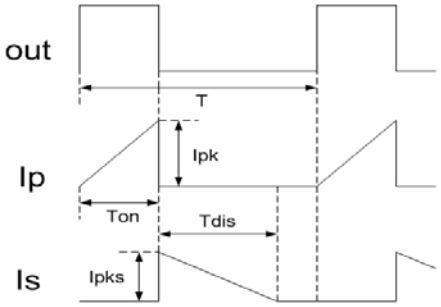


Figure 4. Key Waveforms

Frequency Fall-back Mode

When PSR controller works under CV mode, if output current decreases, the operating frequency decreases as well. When output current decreases to zero, the operating frequency reaches its minimum value. The frequency fallback improves efficiency in light load condition and lowers the standby power loss. While reducing operating frequency with decreasing load current, the controller IC also lowers the primary side peak current at the same time. This makes sure the operating frequency is not too low at no load condition, improving the transient response time.

Frequency Dithering Technique

The device has built-in frequency dithering function to ease EMI system design.

Output Voltage and Current Characteristics

Generally speaking, a battery charger has two charging modes, Constant Voltage mode and Constant Current mode. A basic charging characteristic is shown in Figure 5. When battery voltage is very low or close to cut-off voltage of battery, the charger works in constant current mode; when battery voltage reaches its target value, the output charging current gradually decreases and the charger enters Constant Voltage charging mode until the output charging current is reduced to zero.

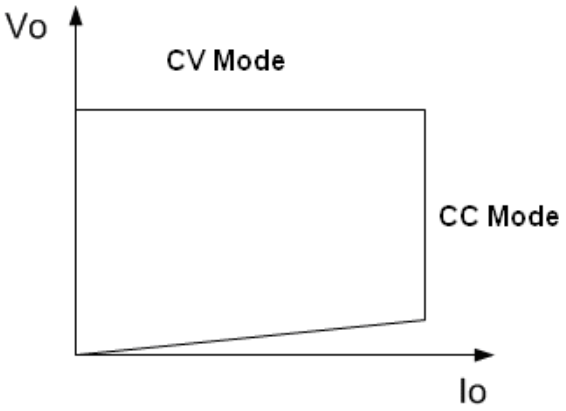


Figure 5. Vo-Io Curve

Start-up Circuit

As shown in Figure 6, when system is powered on with AC voltage, electrolytic capacitor C1 is charged up by Vbus through a start-up resistor R1; once the voltage on Pin Vcc reaches start-up voltage VCC_ON, the controller IC begins to work.

The start-up delay time Tst can be calculated by the below equation 2,

$$T_{st} = -R1 \times C1 \times \ln\left(1 - \frac{V_{CC\_ON}}{\sqrt{2} \times V_{ac} - I_{st} \times R1}\right) \qquad (2)$$

where,

$V_{CC\text{-}ON}$ is the start-up voltage of the device.

Ist is the start-up current of the device.

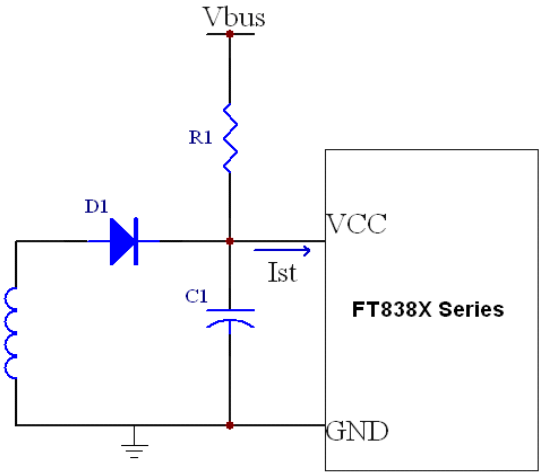


Figure 6. Start-up Circuit

UVLO on Pin VCC

As depicted in Figure 7, the VCC_ON and VCC_OFF of the controller IC are 17.67V and 6.6V, respectively. Once the electrolytic capacitor of VCC C1 is charged up to 17.6V through a start-up resistor R1, and VCC_ON is triggered and the device starts up. C1 provides the energy for the IC before the auxiliary winding starts to supply VCC the voltage above 6.6V. When VCC voltage is less than 6.6V, the device enters Under Voltage Lock Out (UVLO) status, some inner blocks shut down. At this time, the electrolytic capacitor is charged up and the device starts up again when VCC is over 17.6V. The UVLO hysteresis window allows C1 to hold enough charges to supply power for the device at the start up.

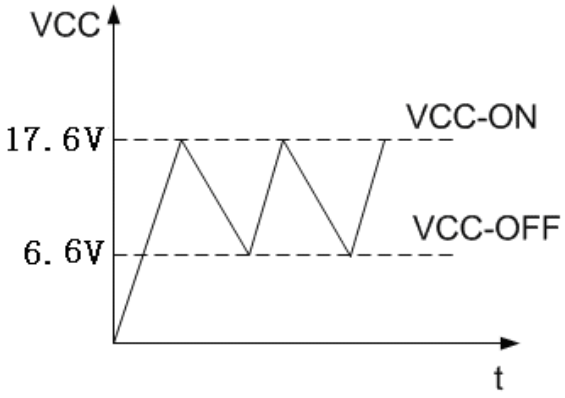


Figure 7. VCC-ON and VCC-OFF

Output Over Voltage and Open Loop Protection

The feedback circuit is shown in Figure 8. The output voltage is fed back to Pin FB by auxiliary winding through resistor divider network formed by resistors R4 and R5. The device regulates the switch off time to keep FB voltage constant at 2.90V.

In the event of resistor R4 open or R5 short or auxiliary winding open, no signal is sensed at Pin FB. The device will shut down the driver output after completing one cycle of operation until the next start-up.

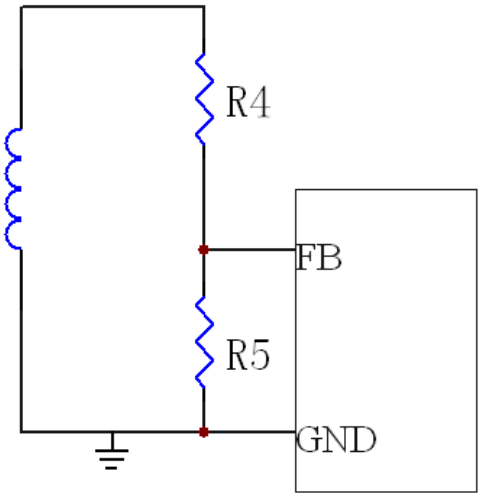


Figure 8. External Circuit for Pin FB

Input AC Brown Out Protection

The device provides input AC Under Voltage Protection, UVP or BOP (Brown Out Protection). As shown in Figure 9, when power NPN Q1 switches on,

$$I_{FB} \approx \frac{V_{bus} \times N_{aux}}{N_P \times R_4} \qquad (3)$$

The current I_{FB} that flows out from Pin FB decreases as input voltage Vbus decreases. When Vbus decreases to certain value causing I_{FB} to be less than the internally set value of 140uA, UVP is triggered and the Out pin will shut down. The VCC voltage will then gradually decrease to the VCC-OFF value. The device then enters the startup process once again.

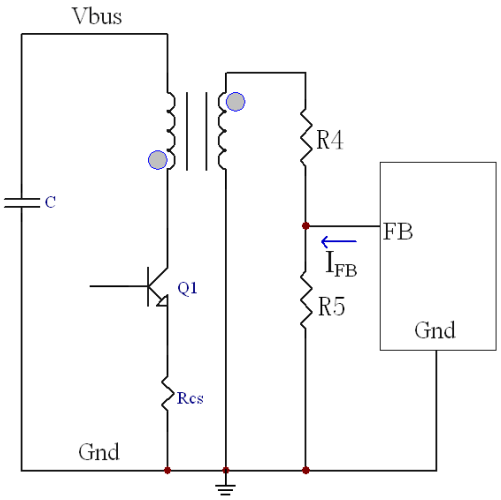


Figure 9. Brown Out Protection

Output Cable Voltage Drop Compensation

Various cable compensation rates are made available to compensate the voltage drop across the output cable. The drop depends on the output cable length and specifications.

If the output voltage is Vout0 at no load condition and the voltage drop across the cable is ΔVout at full load condition, then the required output cable voltage drop compensation ratio is,

Kcab=ΔVout/Vout0

Proper IC part number should be chosen from Table 1 according to the calculated Kcab value.

For example, a 5V / 1.0A charger's output voltage is 5V at no load, and the cable voltage drop is 0.3V when output current is 1.0A at full-load, then Kcab =0.3/5=6%. From Table 1, FT838D2 should be selected.

LEB Time

At the power NPN/MOS turning on instance, current through Rcs will see a spike caused by the reverse recovery current of snubber diode D5, power switch's parasitic capacitor and stray capacitor in primary winding. A 400nS leading-edge blanking (LEB) time is built inside the device to prevent the possible false-trigger caused by the current spike.

Application Information

System Design

Transformer design is the most important step in the process of system design. System working frequency, maximum flux density, and system working mode are all major considerations during transformer design. An example of 5V1.0A system design for charger application is given below to illustrate the design steps and the use of the Excel spreadsheet.

The parameters used in the design and their symbols are described below:

Vac_min：Minimum AC input voltage
Vac_max：Maximum AC input voltage
Vdc_min：Minimum DC input voltage
Vdc_max：Maximum DC input voltage
C1：Main input bulk Ecap
T：Switching period
f：Working frequency
FL：Line frequency for AC input
Ton：Conduction time for power switch
Tdis：Discharging time for secondary winding
L： Inductance for primary winding
Ls：Inductance for secondary winding
Ipk：Peak current for primary winding
Ipks：Peak current for secondary winding
Np：Primary winding turn
Ns：Secondary winding turn
Naux：Auxiliary winding turn
Nps：Ratio of primary and secondary winding
Vo：Output voltage
Io：Output current
V_D：Forward voltage drop for output diode
Vs：Sum of Vo and V_D
Vaux：Supply voltage on auxiliary winding
η：Transformer transferring efficiency
K： A constant parameter built-in the device
Rcs：Primary side sensing resistor
Vcsth：Limiting value on voltage across Rcs

1. Set the Key Known Parameters

AC input voltage
Vac_min=90V，Vac_max=265V；
Line voltage frequency FL=50Hz；
Output: Vo=5V，Io=1A;
System working frequency f=60KHz；
Constant current coefficient K=4 (fixed inside the device)
Ferrite core type: EE16；
Cross section area：AE =19.2mm^2；
Maximum flux density：Bm=270mT；
Auxiliary winding supply voltage：Vaux=11V；
Filling in the Input Section of Excel design form with above given parameters.

Input Section				
Basic Para.	Value	Unit	Discription	Remark
Vac_min	90	V	Min. input voltage (AC)	
Vac_max	265	V	Max. input voltage (AC)	
FL	50	Hz	Line frequency	
η	75	%	System efficiency	
Vout	5	V	Output voltage	
Iout	1	A	Output current	
Fsw	60	KHz	Max. Switching Freq.	1. For BJT: 40-60KHz is recommended. 2. For MOSFET: 60-85KHz is recommended.
Ferrite Core	EE16		Select from Sheet"Ferrite Cores and Bobbins"	
Ae	19.2	mm2	Cross Sectional Area of Core	
Bm	270	mT	Max. Magnetic flux density	250~280mT is recommended
Vaux	11	V	VCC supply voltage	11~18V is recommended
Kcab	6	%	Cable compensation ra	1. For charger: Choose it as per different cable size. 2.For LED Driver: please fill in zero.

Table 3：Input Section Information

2. Determine Input Bulk Ecap

Generally speaking, for universal input range from 90Vac to 264Vac, input bulk electrolytic capacitor value depends on input power value; its typical value is 2~3uF per Watt. Output is 5V 1A, that is 5Watts in total. From the calculated result by the Excel spreadsheet, the recommended value is 11.8uF, 2pcs of 6.8uF are chosen, which is 13.6uF. Therefore, figure 13.6 is filled in C1 as Corrective Value.

3. Determine minimum DC Voltage Vdc_min and maximum DC Voltage Vdc_max

From Figure 10 shown below, the charging time from AC power to C1 through the bridge diode is about 2.8~ 3.3mS (Tc), a typical value of 3.0mS is chosen. Therefore, Vdc min is obtained from below formula,

$$V_{dc\_min} = \sqrt{2 \times V_{ac\_min}^{\ 2} - \frac{2 \times V_O \times I_O \times (\frac{1}{2 \times FL} - T_c)}{\eta \times C_{bulk}}} \quad (5)$$

$$= \sqrt{2 \times 90^2 - \frac{2 \times 5 \times 1 \times (10-3)}{0.75 \times 13.6 \times 10^{-6} \times 1000}}$$

=96.5V

Maximum DC Voltage Vdc_max is then obtained,

$$V_{dc\_max} = \sqrt{2} \times V_{ac\_max} = 371 \ \ V \quad (6)$$

The Excel spreadsheet calculates the above results automatically.

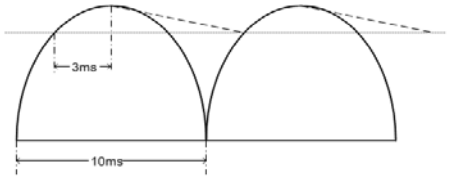


Figure 10. Input DC Voltage Waveform (Dotted Line)

4. Determine Maximum Turn Ratio

The device is designed for flyback topology under DCM. Therefore, to make sure that system works in DCM, the below condition needs to be satisfied. Figure 11 shows the key waveforms that illustrate the condition.

$$T \geq T_{on} + T_{dis} \quad (7)$$

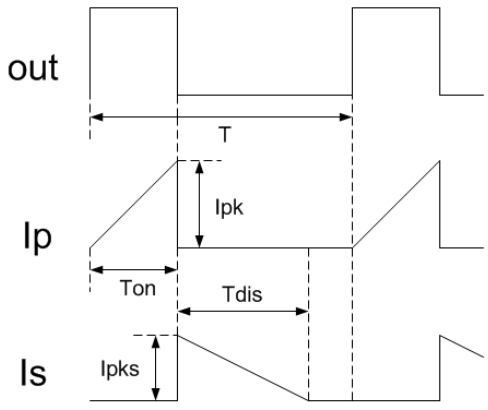


Figure 11. Key Waveforms

Equation (7) translates into

$$N_{ps} \leq V_{dc\_min} \times (\frac{\eta \times K}{2 \times V_O} - \frac{1}{V_O + V_D}) \quad (8)$$

$$= 96.5 \times (\frac{0.75 \times 4}{2 \times 5} - \frac{1}{5 + 0.7}) = 12.02$$

In order to guarantee the system to work in DCM, the chosen Nps shall not be larger than above calculated value. Here we choose Nps = 12.

5. Calculating Peak Current for Primary Winding and Current Sensing Resistor Rcs

From below formulas,

$$I_{pks} = I_{pk} \times N_{ps} \quad (9)$$

$$I_O = \frac{T_{dis} \times I_{pks}}{2 \times T} \quad (10)$$

$$K = \frac{2 \times T}{T_{dis}} = 4 \quad (11)$$

It can be shown:

$$I_{pk} = \frac{K \times I_O}{N_{ps}} = \frac{4 \times 1}{12} = 0.333A \quad (12)$$

Therefore, the sensing resistor is,

$$R_{cs} = \frac{V_{csth}}{I_{pk}} = \frac{0.55}{0.333} = 1.65\Omega \quad (13)$$

where, Vcsth is set internally by the device as 0.55V.

After Rcs is chosen as 1.65 Ohm, Ipk can be re-calculated as:

$$I_{pk} = \frac{0.55}{1.65} = 0.333A$$

6. Determine the Primary Winding Inductance

The primary winding inductance can be calculated from below formula,

$$L = \frac{2 \times P_{in}}{\eta \times I_{PK}^{\ 2} \times f} \quad (14)$$

$$= \frac{2 \times 5 \times 1}{0.75 \times 0.333^2 \times 60 \times 10^3} = 2mH$$

7. Determine Primary Winding Turn

The primary winding turn can be obtained with the known Bm value:

$$N_P = \frac{L \times I_{pk}}{AE \times B_m} = \frac{2.0 \times 333}{19.2 \times 0.27} = 128 \qquad (15)$$

where, AE is ferrite core's cross section area.

8. Calculating Secondary Winding Turn Ns and Auxiliary Winding Turn Naux

Secondary winding turn is,

$$N_s = \frac{N_P}{N_{ps}} = \frac{128}{12} \approx 11 \qquad (16)$$

Auxiliary winding turn is,

$$N_{aux} = N_s \times \frac{V_{aux}}{V_O + V_D} \qquad (17)$$

$$= 11 \times \frac{10}{5 + 0.7} \approx 19$$

9. Determine FB Sampling Resistor R4 and R5

The device provides line compensation through R4 as illustrated in Figure 8. While R4 approaches

$$R_4 = \frac{\sqrt{2} \times V_{ac\_\max} \times N_{aux}}{N_P \times 2 \times 10^{-3}} \qquad (18)$$

$$= \frac{\sqrt{2} \times 264 \times 19}{128 \times 2 \times 10^{-3}} \approx 27K\Omega,$$

the optimal line compensation is obtained, Therefore, R4 value is determined from above equation (18). From Figure 9 we have,

$$\frac{(V_O + V_D) \times N_{aux}}{N_s} = \frac{V_{FB} \times (R_4 + R_5)}{R_5} \qquad (19)$$

where, V_{FB} = 2.9V is an internal value of the device. Hence, R5 can be obtained from below equation (20).

$$R_5 = \frac{R_4 \times N_s \times V_{FB}}{N_{aux} \times (V_O + V_D) - N_s \times V_{FB}} \qquad (20)$$

$$= \frac{27 \times 10^3 \times 11 \times 2.9}{19 \times (5 + 0.7) - 11 \times 2.9} = 11.3K\Omega$$

Design Form-Excel Format

To facilitate the system design, FMD provides the design form with Excel format. Minor changes for individual parameters are made per practical experiences. Design result is shown below.

Output Section					
Basic Para.	Calculated	Correction	Unit	Discription	Remark
Cin	11.8	13.6	uF	Input Bulk E-capacitor	1. For universal input:2~3uF/watt 2. For 180~264Vac: 1uF/watt
Vdc_min	96.5	96.5	V	Min. DC input voltage	"Correction" shall be more than 75V
Nps_max	12.02	12		Max. ratio of NP and NS	"Correction" digit shall be smaller than "Calculated"
Ipk	0.333	0.337	A	Primary peak current	"Correction" digit is decided by Rcs
Rcs	1.67	1.65	Ω	Sensing resistor for primary side	
Lm	1.96	2	mH	Inductance	
Np_min	130.0	128	T	Primary winding turns	
Ns	11	11	T	Secondary winding turns	
Na	22.6	19	T	Auxiliary winding turns	
R4	27.81	27	KΩ	Pull-up resistor for FB divide	The min. resistance cannot be less than 15KOhm.
R5	11.86	11.3	KΩ	Pull-down resistor for FB divider	
Vce_max	441	441	V	Max. peak voltage of Switch	Spike voltage caused by leakage inductance is not included
VD7	37	37	V	Max. reverse voltage for output diode	Derate by 10%
VD6	69	69	V	Max. reverse voltage for Vcc rectified diode	Derate by 10%
R1	2	2	MΩ	Start-up resistor	2MOhm resistor is recommended
C2	10	10	uF	Filter capacitor for VCC sup	4.7uF~10uF E-cap
R9	1.2	1.80	KΩ	Dummy load	Choose as per different application

Verification Section				
Parameter	Expected	Finalized	Unit	Description
Vout	5	5.3	V	Which is direct propotional to R4/R5, Ns/NA
Iout	1	1.02	A	Which is direct propotional to Nps, Ipk
Vaux	11	9.66	V	Which is direct propotional toVout, Na/Ns
Fsw	60	59.66	KHz	Which is direct propotional to Fin and inverse propotional to Lm,Ipk
Bm	270	274.23	mT	The finalized value cannot be more than 300mT
Nps_max	12.0	11.6		The finalized value cannot be more than expected value

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