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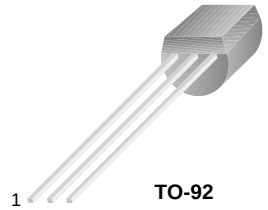
March 2013

KSD471A
NPN Epitaxial Silicon Transistor

Features

- Audio Frequency Power Amplifier
- Complement to KSB564A
- Collector Current: I_C = 1 A
- Collector Power Dissipation: P_C = 800 mW
- Suffix "-C" means Center Collector
  (1. Emitter 2. Collector 3. Base)



TO-92

1. Emitter 2. Base 3. Collector

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Ratings	Unit
V_{CBO}	Collector-Base Voltage	40	V
V_{CEO}	Collector-Emitter Voltage	30	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	1	A
P_C	Collector Power Dissipation	800	mW
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	-55 to +150	°C

Electrical Characteristics

Values are at T_A = 25°C unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
BV_{CBO}	Collector-Base Breakdown Voltage	I_C = 100 μA, I_E = 0	40			V
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 10 mA, I_B = 0	30			V
BV_{EBO}	Emitter-Base Breakdown Voltage	I_E = 100 μA, I_C = 0	5			V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30 V, I_E = 0			0.1	μA
h_{FE}	DC Current Gain	V_{CE} = 1 V, I_C = 100 mA	120		400	
V_{CE} (sat)	Collector-Emitter Saturation Voltage	I_C = 1 A, I_B = 0.1 A			0.5	V
V_{BE} (sat)	Base-Emitter Saturation Voltage	I_C = 1 A, I_B = 0.1 A			1.2	V
f_T	Current Gain BandWidth Product	V_{CE} = 6 V, I_C = 10 mA		130		MHz
C_{ob}	Output Capacitance	V_{CB} = 6 V, I_E = 0, f = 1 MHz		16		pF

h_{FE} Classification

Classification	Y	G
h_{FE}	120 ~ 240	200 ~ 400

Typical Performance Characteristics

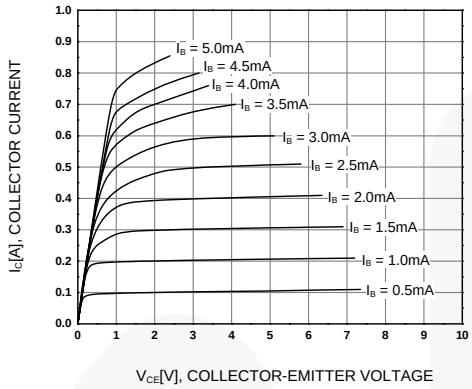


Figure 1. Static Characteristic

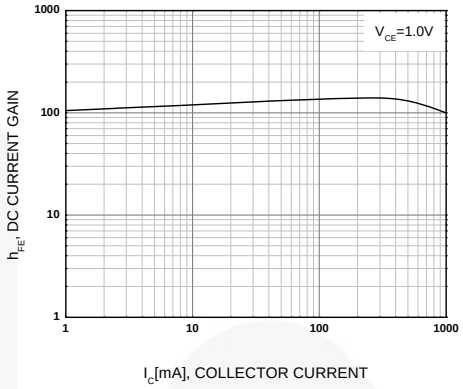


Figure 2. DC current Gain

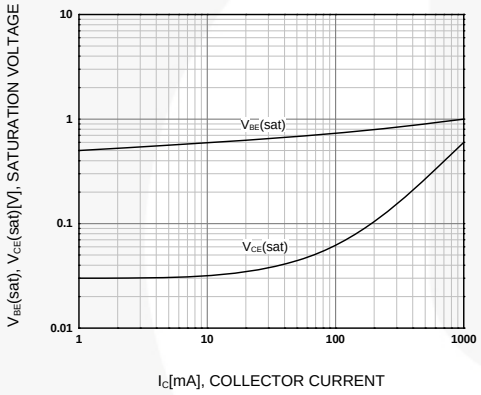


Figure 3. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

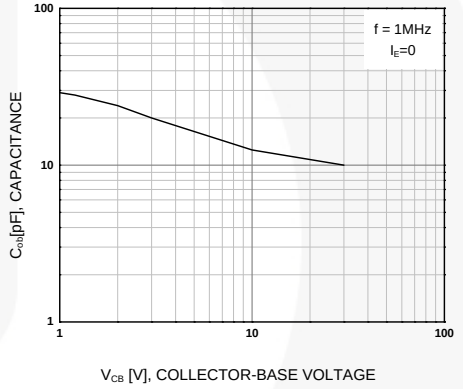


Figure 4. Collector Output Capacitance

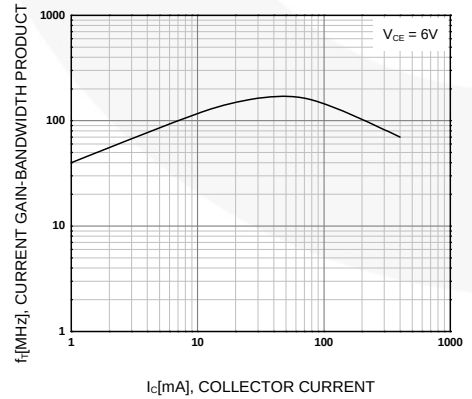


Figure 5. Current Gain Bandwidth Product

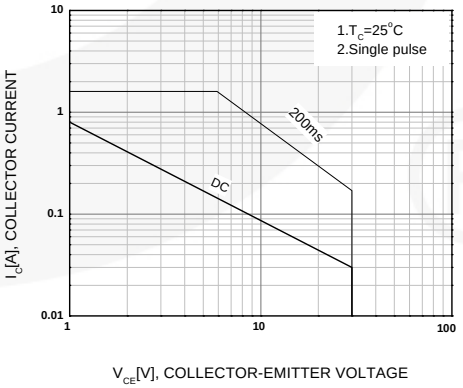
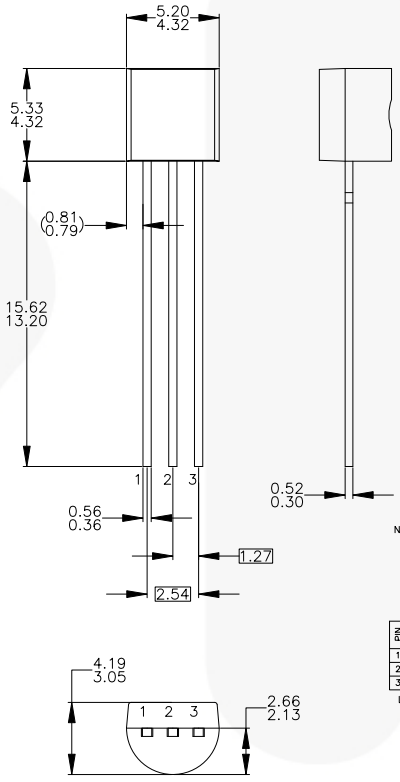


Figure 6. Safe Operating Area

Physical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DRAWING CONFORMS TO ASME Y14.5M-1994.
D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	P	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P – BIPOLAR
F – JFET
M – DMOS
E – EMITTER
B – BASE
C – COLLECTOR
D – DRAIN
S – SOURCE
G – GATE

E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEAGLE AT JFET "F" OPTION.
F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 7. 3LEAD, TO92, JEDEC TO-92 COMPLIANT STRAIGHT LEAD CONFIGURATION (OLD TO92AM3)

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