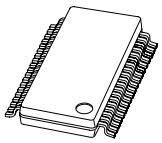


# IP4778CZ38

## HDMI ESD protection, DDC buffering and hot plug control

Rev. 3 — 31 March 2011 Product data sheet

## 1. General description

The IP4778CZ38 is designed for HDMI receiver host interface protection.
The IP4778CZ38 includes DDC buffering, slew rate acceleration and decoupling, hot plug control, backdrive protection, CEC slew rate control, optional multiplexing of DDC signals, and high-level ESD protection diodes for all HDMI signals.

The DDC lines are buffered using a new buffering concept which decouples the internal capacitive load from the external capacitive load. This allows higher PCB design flexibility for the DDC lines with respect to a maximum load of 50 pF. This buffering also boosts the DDC signals, allowing the use of longer HDMI cables having a higher capacitive load than 700 pF. The CEC slew rate limiter prevents ringing on the CEC line and greatly reduces the number of discrete components needed by the CEC application. HDMI receiver and system GPIO applications are simplified by an internal hot plug driver module and hot plug control.

The DDC, hot plug and CEC lines are backdrive protected to guarantee HDMI interface signals are not pulled down if the system is powered down or enters Standby mode.

All TMDS intra-pairs are protected by a special diode configuration offering a low line capacitance of 0.7 pF only (to ground) and 0.05 pF between the TMDS pairs. These diodes provide protection to components downstream from ESD voltages of up to ±8 kV contact in accordance with the IEC 61000-4-2, level 4 standard.

## 2. Features and benefits

- Pb-free and RoHS compliant
- Robust ESD protection without degradation after several ESD strikes
- Low leakage even after several hundred ESD discharges
- Very high diode switching speed (ns) and low line capacitance of 0.7 pF to ground and 0.05 pF between channels ensures signal integrity
- DDC capacitive decoupling between system side and HDMI connector side and drive cable buffering with capacitive load (> 700 pF)
- Hot plug control for direct connection to system GPIO
- CEC ringing prevention by slew rate limiter
- DDC and hot plug enable signal for multiplexing and backdrive protection
- All TMDS lines with integrated rail-to-rail clamping diodes with downstream ESD protection of ±8 kV in accordance with IEC 61000-4-2, level 4
- Matched 0.5 mm trace spacing
- Component count reduction of HDMI receiver application

- Highest integration in a small footprint, PCB level, optimized RF routing, 38-pin TSSOP lead-free package
- Choice of system compatible or RF routing optimized pinning variants

## 3. Applications

- The IP4778CZ38 can be used for a wide range of HDMI sink devices e.g.:
  - TV
  - Projectors
  - PC monitors
  - HDMI buffer modules (extensions of HDMI cable length)
  - HDMI picture performance quality enhancer modules

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| IP4778CZ38 | TSSOP38 | plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm | SOT510-1 |
| IP4778CZ38/V | | | |

## 5. Functional diagram

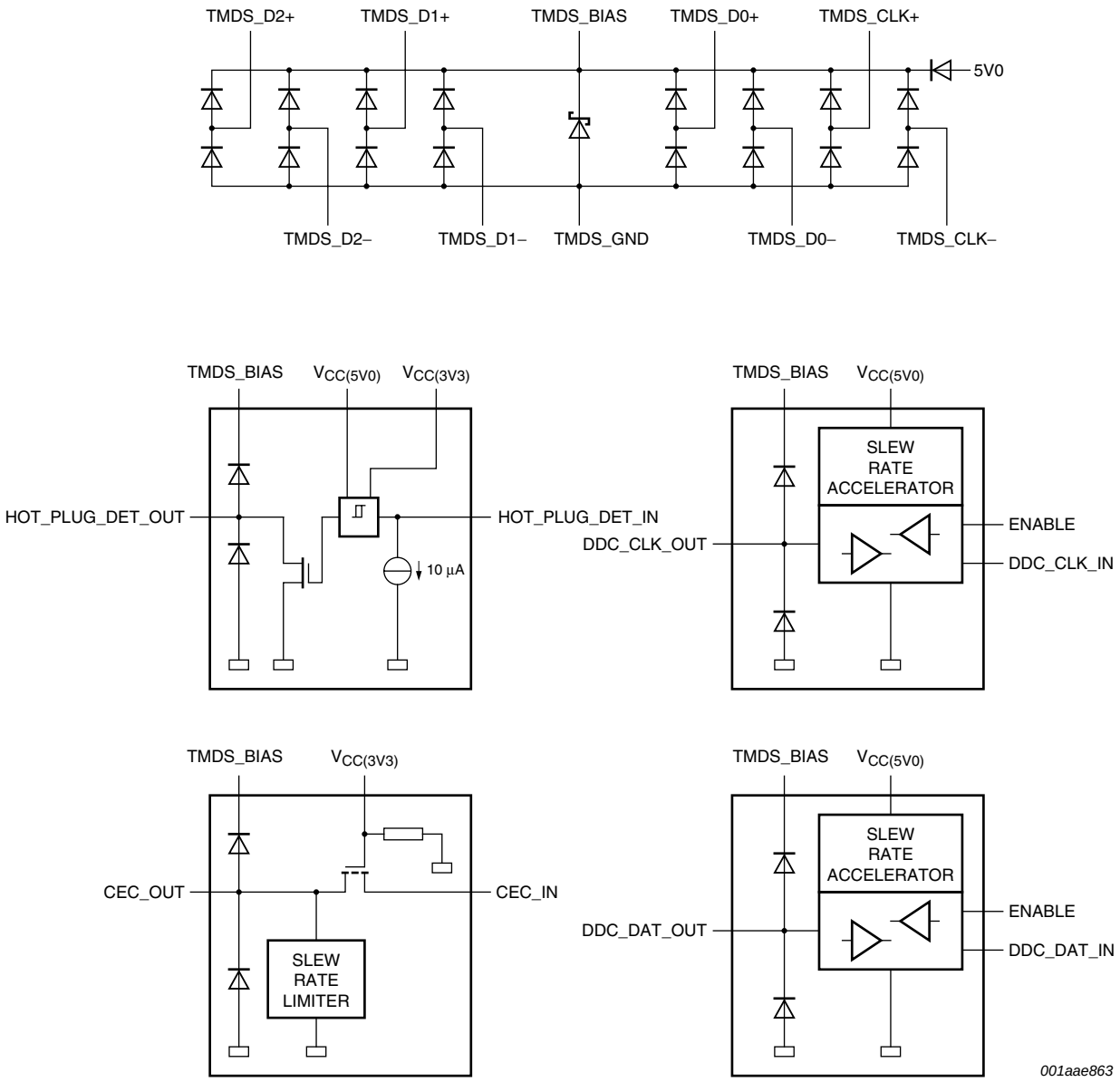



**Fig 1. Functional diagram**

# 6. Pinning information

## 6.1 Pinning

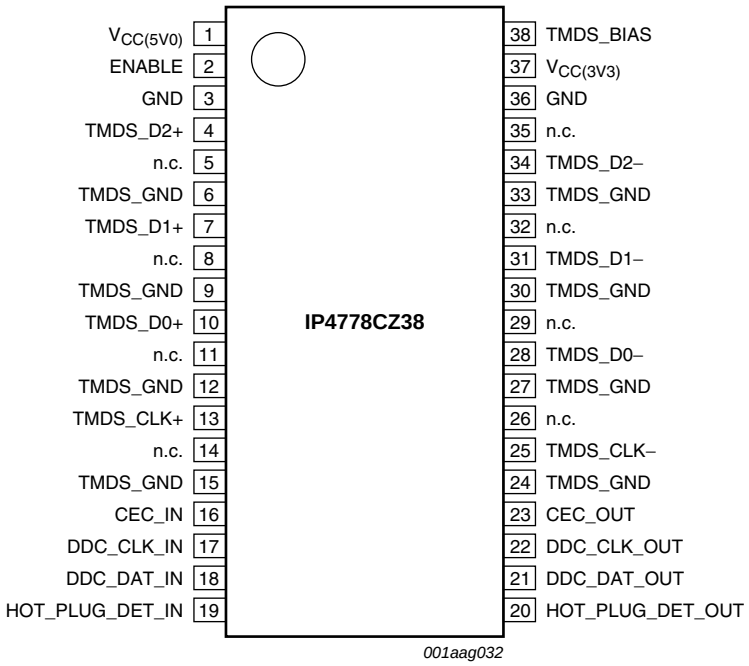



**Fig 2. Pin configuration of IP4778CZ38**

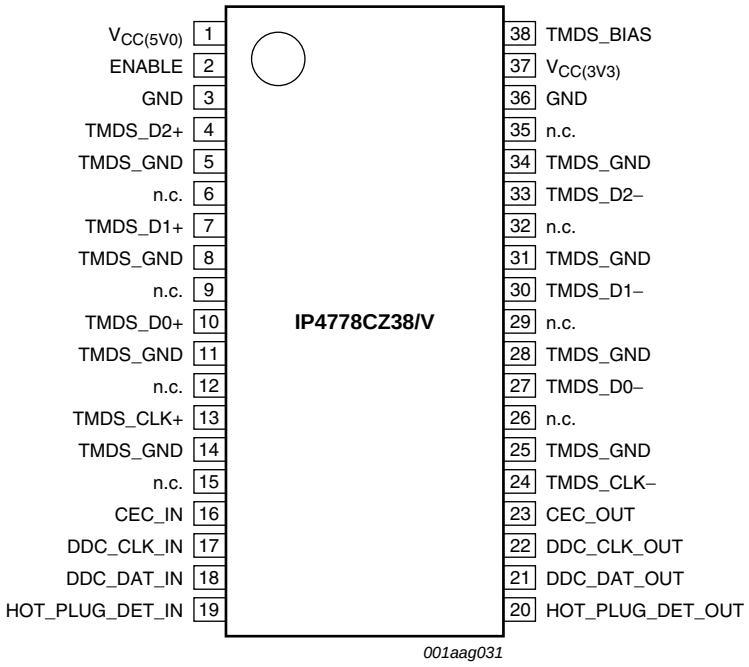



**Fig 3. Pin configuration of IP4778CZ38/V**

## 6.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | | Description |
|---|---|---|---|
| | IP4778CZ38 | IP4778CZ38/V | |
| $V_{CC(5V0)}$ | 1 | 1 | supply voltage for DDC and hot plug circuits |
| ENABLE | 2 | 2 | enable for DDC and hot plug circuits |
| GND | 3 | 3 | ground for DDC, hot plug and CEC circuits[1] |
| TMDS_D2+ | 4 | 4 | ESD protection TMDS channel D2+[2] |
| TMDS_GND | 6 | 5 | ground for TMDS channel[1] |
| n.c. | 5 | 6 | not connected[2] |
| TMDS_D1+ | 7 | 7 | ESD protection TMDS channel D1+[2] |
| TMDS_GND | 9 | 8 | ground for TMDS channel[1] |
| n.c. | 8 | 9 | not connected[2] |
| TMDS_D0+ | 10 | 10 | ESD protection TMDS channel D0+[2] |
| TMDS_GND | 12 | 11 | ground for TMDS channel[1] |
| n.c. | 11 | 12 | not connected[2] |
| TMDS_CLK+ | 13 | 13 | ESD protection TMDS channel CLK+[2] |
| TMDS_GND | 15 | 14 | ground for TMDS channel[1] |
| n.c. | 14 | 15 | not connected[2] |
| CEC_IN | 16 | 16 | CEC signal input to system controller[3] |
| DDC_CLK_IN | 17 | 17 | DDC clock input to system controller[3] |
| DDC_DAT_IN | 18 | 18 | DDC data input to system controller[3] |
| HOT_PLUG_DET_IN | 19 | 19 | hot plug Detect input from system GPIO[3] |
| HOT_PLUG_DET_OUT | 20 | 20 | hot plug Detect output to HDMI connector[4] |
| DDC_DAT_OUT | 21 | 21 | DDC data output to HDMI connector[4] |
| DDC_CLK_OUT | 22 | 22 | DDC clock output to HDMI connector[4] |
| CEC_OUT | 23 | 23 | CEC signal output to HDMI connector[3] |
| TMDS_CLK– | 25 | 24 | ESD protection TMDS channel CLK–[2] |
| TMDS_GND | 24 | 25 | ground for TMDS channel[1] |
| n.c. | 26 | 26 | not connected[2] |
| TMDS_D0– | 28 | 27 | ESD protection TMDS channel D0–[2] |
| TMDS_GND | 27 | 28 | ground for TMDS channel[1] |
| n.c. | 29 | 29 | not connected[2] |
| TMDS_D1– | 31 | 30 | ESD protection TMDS channel D1–[2] |
| TMDS_GND | 30 | 31 | ground for TMDS channel[1] |

**Table 2. Pin description** *...continued*

| Symbol | Pin | | Description |
|---|---|---|---|
| | IP4778CZ38 | IP4778CZ38/V | |
| n.c. | 32 | 32 | not connected[2] |
| TMDS_D2– | 34 | 33 | ESD protection TMDS channel D2–[2] |
| TMDS_GND | 33 | 34 | ground for TMDS channel[1] |
| n.c. | 35 | 35 | not connected[2] |
| GND | 36 | 36 | ground for DDC, hot plug and CEC circuits[1] |
| $V_{CC(3V3)}$ | 37 | 37 | supply voltage for CEC circuit |
| TMDS_BIAS | 38 | 38 | bias input for TMDS ESD protection. This pin must be connected to a 0.1 μF capacitor. |

[1] Pins GND and TMDS_GND are internally connected.

[2] This pin must always be connected to the IC pin located opposite via a PCB track to guarantee correct functionality; see Figure 15.

[3] $V_{CC(3V3)}$ referenced logic level in.

[4] $V_{CC(5V0)}$ referenced logic level out.

# 7. Limiting values

**Table 3. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | GND – 0.5 | 5.5 | V |
| $V_I$ | input voltage | at input pins | | GND – 0.5 | 5.5 | V |
| $V_{ESD}$ | electrostatic discharge voltage | connector side pins (to ground); IEC 61000-4-2, level 4 | [1] | | | |
| | | contact | | –8 | +8 | kV |
| | | board side pins; IEC 61000-4-2, level 1 | [2] | | | |
| | | contact | | –2 | +2 | kV |
| $P_{tot}$ | total power dissipation | DDC operating at 100 kHz | | - | 8 | mW |
| $T_{stg}$ | storage temperature | | | –55 | +125 | °C |

[1] Connector side pins:
TMDS_D2+, TMDS_D2–, TMDS_D1+, TMDS_D1–, TMDS_D0+, TMDS_D0–,
TMDS_CLK+, TMDS_CLK–,
CEC_OUT,
DDC_DAT_OUT and DDC_CLK_OUT,
HOT_PLUG_DET_OUT.

[2] Board side pins:
CEC_IN,
DDC_DAT_IN and DDC_CLK_IN,
HOT_PLUG_DET_IN,
ENABLE.

# 8. Static characteristics

**Table 4. TMDS protection circuit**

*$T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Zener diode** | | | | | | | |
| $V_{BRzd}$ | Zener diode breakdown voltage | I = 1 mA | | 6 | - | 9 | V |
| $R_{dyn}$ | dynamic resistance | I = 1 A; IEC 61000-4-5/9 | | | | | |
| | | positive transient | | - | 2.4 | - | Ω |
| | | negative transient | | - | 1.3 | - | Ω |
| **Protection diode** | | | | | | | |
| $I_{bck}$ | back current | from pins TMDS_x to pin TMDS_BIAS; $V_{CC(5V0)}$ = 0 V; $V_{CC(3V3)}$ = 0 V | | - | 0.1 | 5 | μA |
| $I_{L(r)}$ | reverse leakage current | $V_I$ = 3.0 V | | - | 1 | - | μA |
| $V_F$ | forward voltage | | | - | 0.7 | - | V |
| $V_{CL(ch)trt(pos)}$ | positive transient channel clamping voltage | $V_{ESD}$ = 8 kV per IEC 61000-4-2; voltage 30 ns after trigger | [1] | - | 8 | - | V |
| **TMDS channel: pins TMDS_x** | | | | | | | |
| $C_{ch(TMDS)}$ | TMDS channel capacitance | $V_{CC(5V0)}$ = 5 V; f = 1 MHz; $V_{bias}$ = 2.5 V | [2] | - | 0.7 | - | pF |
| $\Delta C_{ch(TMDS)}$ | TMDS channel capacitance difference | $V_{CC(5V0)}$ = 5 V; f = 1 MHz; $V_{bias}$ = 2.5 V | [2] | - | 0.05 | - | pF |
| $C_{ch(mutual)}$ | mutual channel capacitance | between signal pin TMDS_x and pin n.c.; $V_{CC(5V0)}$ = 0 V; f = 1 MHz; $V_{bias}$ = 2.5 V | [2] | - | 0.07 | - | pF |

[1] This measurement is performed with a 0.1 μF external capacitor on pin TMDS_BIAS.

[2] This parameter is guaranteed by design.

**Table 5. DDC circuit**

*$V_{CC(3V3)}$ = 2.7 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 5.5 V; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supplies: pins $V_{CC(5V0)}$ and $V_{CC(3V3)}$** | | | | | | |
| $V_{CC(5V0)}$ | supply voltage (5.0 V) | | 4.5 | 5.0 | 5.5 | V |
| $V_{CC(3V3)}$ | supply voltage (3.3 V) | | 2.7 | 3.3 | 5.5 | V |
| $I_{CC(5V0)}$ | supply current (5.0 V) | $V_{CC(5V0)}$ = 5.5 V; both channels HIGH: DDC_DAT_OUT = $V_{CC(5V0)}$; DDC_CLK_OUT = $V_{CC(5V0)}$ | - | 0.5 | 1.0 | mA |
| | | $V_{CC(5V0)}$ = 5.5 V; both channels LOW: DDC_DAT_IN = GND; DDC_CLK_IN = GND; DDC_DAT_OUT = open; DDC_CLK_OUT = open | - | 0.5 | 1.0 | mA |
| $I_{CC(3V3)}$ | supply current (3.3 V) | no pull-up resistor connected to $V_{CC(3V3)}$ | - | - | 0.1 | μA |

**Table 5. DDC circuit** *…continued*

*$V_{CC(3V3)}$ = 2.7 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 5.5 V; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Board side: pins DDC_CLK_OUT and DDC_DAT_OUT** | | | | | | |
| Used as input | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | $0.7 \times V_{CC(3V3)}$ | - | 5.5 | V |
| $V_{IL}$ | LOW-level input voltage | | −0.5 | - | $0.3 \times V_{CC(3V3)}$ | V |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.2 V | - | - | 1 | μA |
| $V_{IK}$ | input clamping voltage | $I_i$ = −18 mA | - | - | −1.2 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 3.6 V | - | - | ±1 | μA |
| $C_i$ | input capacitance | $V_I$ = 3 V or 0 V | | | | |
| | | $V_{CC(3V3)}$ = 3.3 V | - | 8 | 10 | pF |
| | | $V_{CC(3V3)}$ = 3.0 V | - | 8 | 10 | pF |
| Used as output | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 100 μA or 6 mA | - | 200 | - | mV |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 3.6 V | - | - | 1 | μA |
| $C_o$ | output capacitance | $V_I$ = 3 V or 0 V | | | | |
| | | $V_{CC(3V3)}$ = 3.3 V | - | 8 | 10 | pF |
| | | $V_{CC(3V3)}$ = 3.0 V | - | 8 | 10 | pF |
| **Connector side: pins DDC_CLK_IN and DDC_DAT_IN** | | | | | | |
| Used as input | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | - | 410 | - | mV |
| $V_{IL}$ | LOW-level input voltage | | - | 400 | - | mV |
| $I_{IL}$ | LOW-level input current | DDC_DAT_OUT, DDC_CLK_OUT, $V_I$ = 0.2 V | - | - | 10 | μA |
| $V_{IK}$ | input clamping voltage | $I_I$ = −18 mA | - | - | −1.2 | V |
| $I_{LI}$ | input leakage current | $V_I$ = 3.6 V | - | - | ±1 | μA |
| $C_i$ | input capacitance | $V_I$ = 3 V or 0 V | | | | |
| | | $V_{CC(3V3)}$ = 3.3 V | - | 7 | 9 | pF |
| | | $V_{CC(3V3)}$ = 3.0 V | - | 7 | 9 | pF |
| Used as output | | | | | | |
| $V_{OL}$ | LOW-level output voltage | $I_{OL}$ = 100 μA or 3 mA | - | 700 | - | mV |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 3.6 V | - | - | 1 | μA |
| $C_o$ | output capacitance | $V_I$ = 3 V or 0 V | | | | |
| | | $V_{CC(3V3)}$ = 3.3 V | - | 8 | 10 | pF |
| | | $V_{CC(3V3)}$ = 3.0 V | - | 8 | 10 | pF |

**Table 6. CEC circuit**

*$V_{CC(3V3)}$ = 2.7 V to 5.5 V; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Board side: input pin CEC_IN** | | | | | | | |
| $C_{I(ch-GND)(levsh)}$ | level shifting input capacitance from channel to ground | $V_{CC(3V3)}$ = 0 V; f = 1 MHz; $V_{bias}$ = 2.5 V | [1] | - | 12 | 16 | pF |
| $SR_r$ | rising slew rate | $V_I$ > 1.8 V | | - | 10 | - | mV/µs |
| **N-FET** | | | | | | | |
| $\Delta V_{on}$ | on-state voltage drop | N-FET state = on; $V_{CC(3V3)}$ = 2.5 V; $V_S$ = GND; $I_{DS}$ = 3 mA | [2] | - | 125 | 140 | mV |
| **Connector side: output pin CEC_OUT** | | | | | | | |
| $I_{LI}$ | input leakage current | | | −1 | +0.1 | +1 | µA |
| $R_{dyn}$ | dynamic resistance | I = 1 A; IEC 61000-4-5/9 | | | | | |
| | | positive transient | | - | 2.4 | - | Ω |
| | | negative transient | | - | 1.3 | - | Ω |
| $V_{CL(ch)trt(pos)}$ | positive transient channel clamping voltage | $V_{ESD}$ = 8 kV per IEC 61000-4-2; voltage 30 ns after trigger; $T_{amb}$ = 25 °C | [3] | - | 8 | - | V |

[1] This parameter is guaranteed by design.

[2] For level shifting N-FET.

[3] This measurement is performed with a 0.1 µF external capacitor on pin TMDS_BIAS.

**Table 7. Enable circuit**

*$V_{CC(3V3)}$ = 2.7 V to 5.5 V; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Board side: input pin ENABLE[1]** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | HIGH = enable | 0.7 × $V_{CC(3V3)}$ | - | $V_{CC(5V0)}$ + 0.5 | V |
| $V_{IL}$ | LOW-level input voltage | LOW = disable | −0.5 | - | 0.3 × $V_{CC(3V3)}$ | V |
| $I_{IL}$ | LOW-level input current | $V_I$ = 0.2 V; $V_{CC(3V3)}$ = 5.5 V | - | 10 | - | µA |
| $I_{LI}$ | input leakage current | | −1 | +0.1 | +1 | µA |
| $C_i$ | input capacitance | $V_I$ = 3 V or 0 V | - | 3 | 7 | pF |

[1] The ENABLE pin has to be connected permanently to $V_{CC(3V3)}$ if no enable control is needed.

**Table 8. hot plug control circuit**

*$V_{CC(5V0)}$ = 4.5 V to 5.5 V; $V_{CC(3V3)}$ = 2.7 V to 5.5 V; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Board side: input pin HOT_PLUG_DET_IN** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | HIGH = hot plug off | $0.7 \times V_{CC(3V3)}$ | - | $V_{CC(5V0)} + 0.5$ | V |
| $V_{IL}$ | LOW-level input voltage | LOW = hot plug on | −0.5 | - | $0.3 \times V_{CC(3V3)}$ | V |
| $I_{IL}$ | LOW-level input current | $V_I$ = 2.0 V; $V_{CC(3V3)}$ = 5.5 V | - | 10 | - | µA |
| $I_{LI}$ | input leakage current | | −1 | +0.1 | +1 | µA |
| $C_i$ | input capacitance | $V_I$ = 3 V or 0 V | - | 4 | 7 | pF |
| **Connector side: output pin HOT_PLUG_DET_OUT** | | | | | | |
| $I_{LI}$ | input leakage current | | −1 | +0.1 | +1 | µA |
| $C_i$ | input capacitance | $V_I$ = 3 V or 0 V | - | 6 | 7 | pF |
| $V_{on}$ | on-state voltage | $I_I$ = 5 mA | - | 400 | - | mV |

# 9. Dynamic characteristics

**Table 9. DDC circuits**

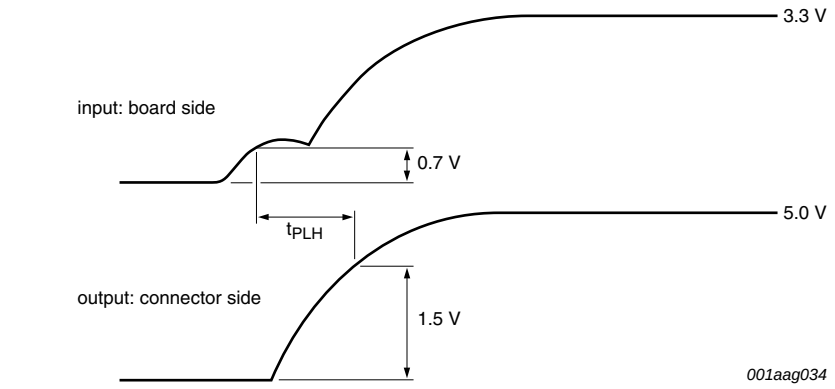
*$V_{CC(3V3)}$ = 2.7 V to 5.5 V; $V_{CC(5V0)}$ = 4.5 V to 5.5 V; GND = 0 V; $T_{amb}$ = 25 °C; unless otherwise specified.*

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Board side to connector side; see Figure 4** | | | | | | | |
| Pins DDC_CLK_IN to DDC_CLK_OUT and DDC_DAT_IN to DDC_DAT_OUT | | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | | [1] | 150 | 270 | 300 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | | [1] | 125 | 210 | 225 | ns |
| Pins DDC_CLK_OUT and DDC_DAT_OUT | | | | | | | |
| $t_{TLH}$ | LOW to HIGH transition time | $R_L$ = 1.35 kΩ; $C_L$ = 50 pF | | 90 | 110 | 130 | ns |
| $t_{THL}$ | HIGH to LOW transition time | | [1] | 2 | 3 | 5 | ns |
| **Connector side to board side; see Figure 5** | | | | | | | |
| Pins DDC_CLK_OUT to DDC_CLK_IN and DDC_DAT_OUT to DDC_DAT_IN | | | | | | | |
| $t_{PLH}$ | LOW to HIGH propagation delay | | | 90 | 110 | 130 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | | [1] | 20 | 30 | 40 | ns |
| Pins DDC_CLK_IN and DDC_DAT_IN | | | | | | | |
| $t_{TLH}$ | LOW to HIGH transition time | | | 100 | 120 | 140 | ns |
| $t_{THL}$ | HIGH to LOW transition time | | [1] | 2 | 3 | 5 | ns |
| **Enable: pin ENABLE** | | | | | | | |
| $t_{su}$ | set-up time | pin ENABLE = HIGH before start condition | [2] | 100 | - | - | ns |
| $t_h$ | hold time | pin ENABLE = HIGH after stop condition | [2] | 100 | - | - | ns |

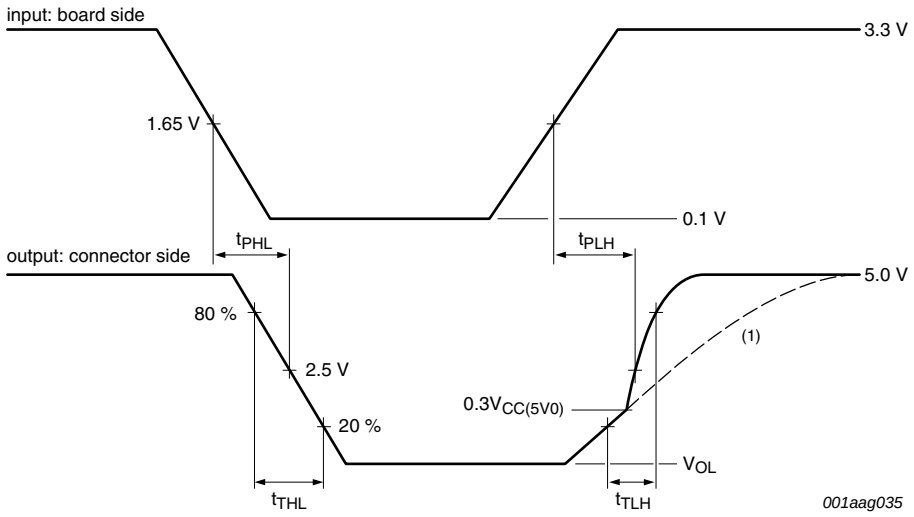
[1] Typical values were measured with $V_{CC(3V3)}$ = 3.3 V; $V_{CC(5V0)}$ = 5.0 V.

[2] Pin ENABLE should only change state when the DDC bus is in an idle state.

## 9.1 AC Waveforms



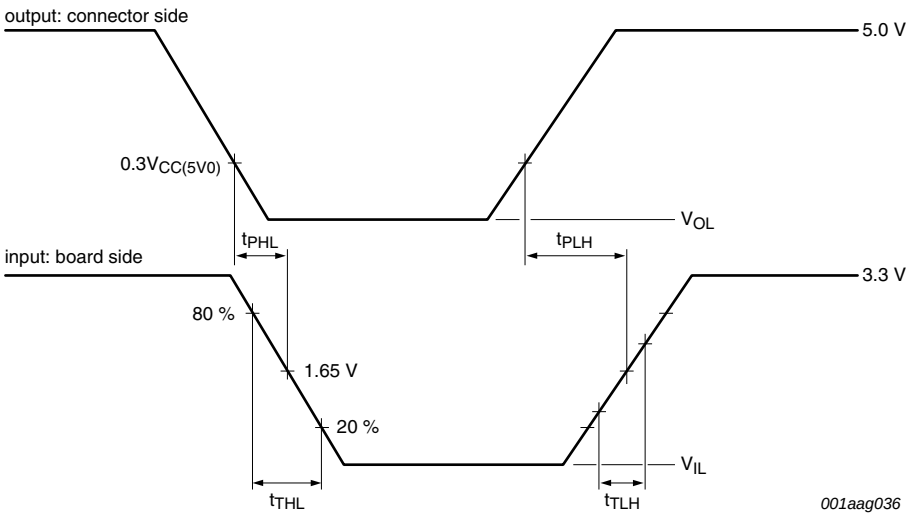

a. Propagation delay $t_{PLH}$




(1) Dotted line indicates effect without slew rate accelerator.

b. Propagation delay $t_{PHL}$ and transition time

**Fig 4. Board side to connector side operation**




Propagation delay output to input and transition time input

**Fig 5. Connector side to board side operation**

# 10. Application information

## 10.1 TMDS

To protect the TMDS lines and also to comply with the impedance requirements of the HDMI specification, the IP4778CZ38 provides ESD protection with a low capacitive load. The dominant value for the TMDS line impedance is the capacitive load to ground. The IP4778CZ38 has a capacitive load of only 0.7 pF.

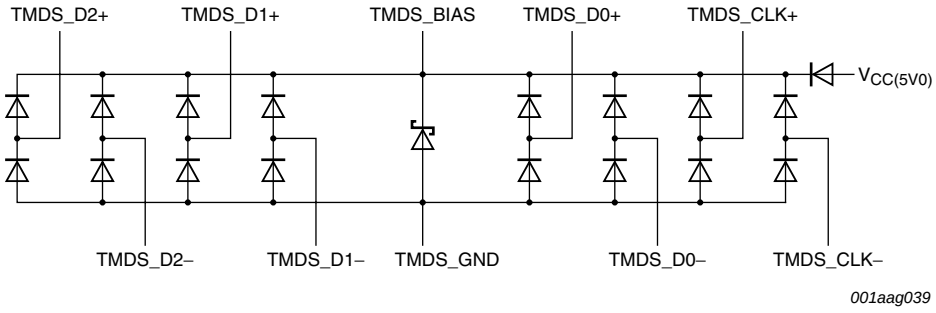


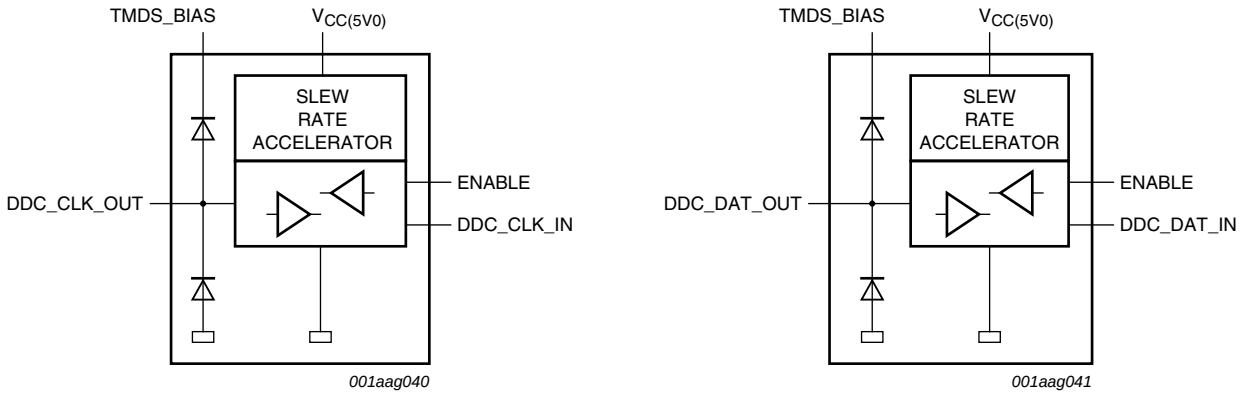

**Fig 6. ESD protection of TMDS lines**

## 10.2 DDC circuit

The DDC-bus circuit contains full capacitive decoupling between the HDMI connector and the DDC-bus lines on the PCB. The capacitive decoupling ensures that the maximum capacitive load is within the 50 pF maximum of the HDMI specification.

The slew rate accelerator supports high capacitive load on the HDMI cable side. Various HDMI cable suppliers produce low-cost and long (typically 25 m) HDMI cables with a capacitive load of up to 6 nF.

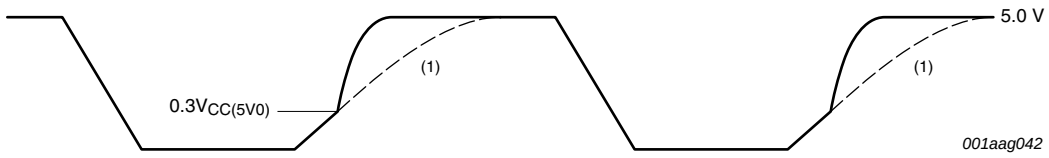
The slew rate accelerator boosts the DDC signal independent of which side of the bus is releasing the signal. The DDC module provides a level shifting and a multiplex option which is enabled by the ENABLE signal.




a. DDC clock

b. DDC data

**Fig 7. DDC circuit**




(1) Dotted line indicates effect without slew rate accelerator.

**Fig 8. DDC output waveform**

## 10.3 Hot plug driver circuit

The IP4778CZ38 includes a hot plug driver circuit that simplifies the hot plug application. The circuit can be connected directly to GPIO pins.

The hot plug control input is actively pulled LOW to ensure that at system standby or start-up, the hot plug signal is HIGH even if a GPIO pin is in a 3-state condition.

For correct CEC handling, it is essential that the hot plug signal is at HIGH-level in Standby mode. The HDMI source requires a hot plug signal so that it can read out the EDID information to initiate a proper start-up CEC sequence.

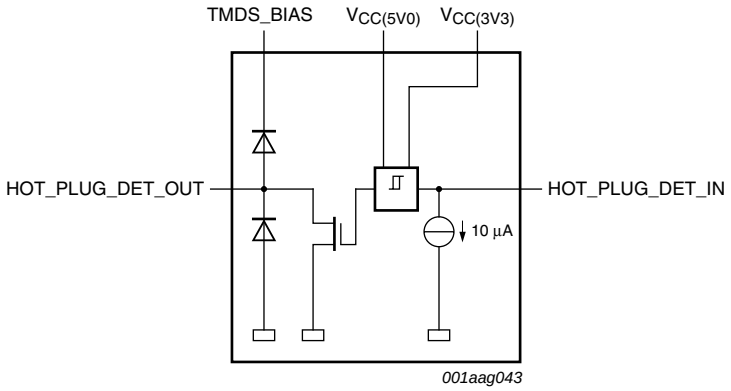



**Fig 9. Hot plug driver circuit**

## 10.4 CEC

The CEC signal can generate distortions caused by signal ringing in a 1 kHz domain. The CEC slew rate limiter ensures that a signal does not ring independently of the CEC slave that is releasing the signal.

A MOSFET transistor implements the backdrive protection which blocks signals during a power-down state.

The slew rate of the CEC bus is controlled by a slew rate that is defined independently of the load (ohmic and capacitive) at the CEC bus.

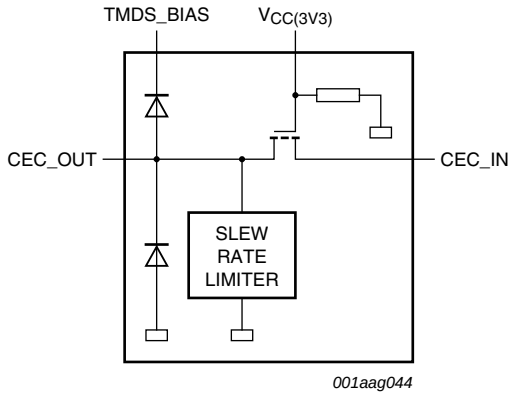
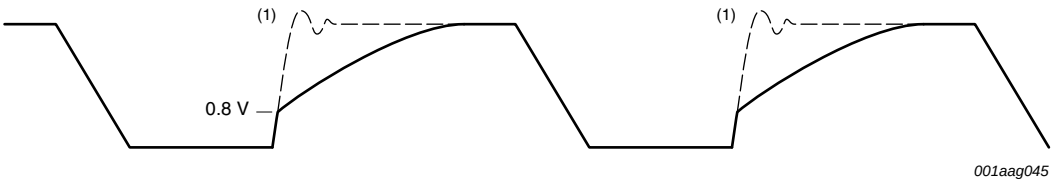



**Fig 10. CEC module**




(1) Dotted line indicates effect without slew rate limiter.

**Fig 11. CEC output waveform**

## 10.5 Multiplexing

Up to four HDMI interface ports can exist on an HDMI receiver. The DDC and hot plug signals are both needed to support various HDMI connectors, multiplexing and switching of the TMDS lines. The CEC bus has to remain functional in order to detect activity such as a brake in support.

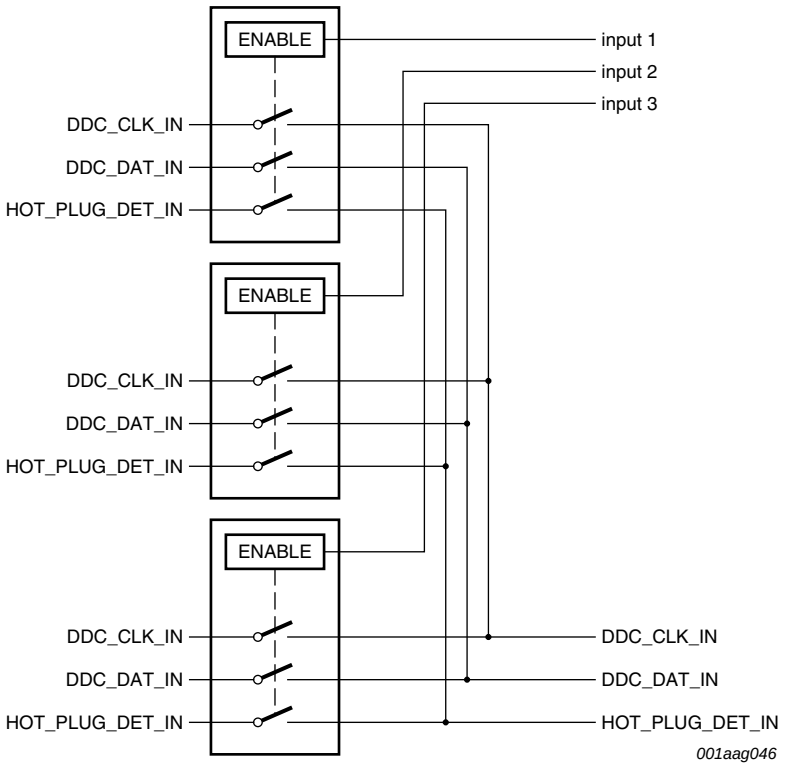



**Fig 12. Example of multiplexing both DDC and hot plug**

The combination of a TMDS switch and the IP4778CZ38 is a cost-effective way to attain various HDMI ports by using a single input HDMI receiver device. The ENABLE signal activates the HDMI DDC and hot plug lines at the port that is selected by the system controller.

## 10.6 Backdrive protection

The HDMI contains various signals which can partly supply current into an HDMI device that is powered down.

Typically, the DDC lines and the CEC signals can force 5 V into the switched-off device. The IP4778CZ38 ensures that at power-down, the critical signals are blocked to prevent any damage to the HDMI sink and HDMI source.

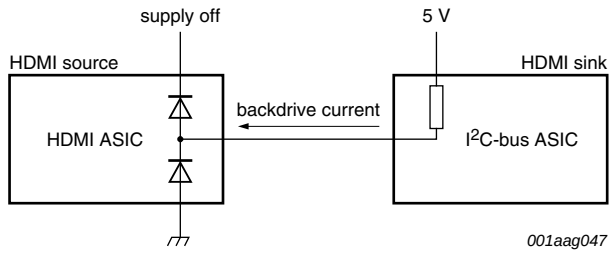



**Fig 13. Backdrive protection**

## 10.7 Application schematic

Figure 14 shows a typical application where the IP4778CZ38 provides a simplified interface to an HDMI port. This application requires only a few external components to adapt the HDMI port to the parameters of the HDMI receiver device or HDMI multiplexer.

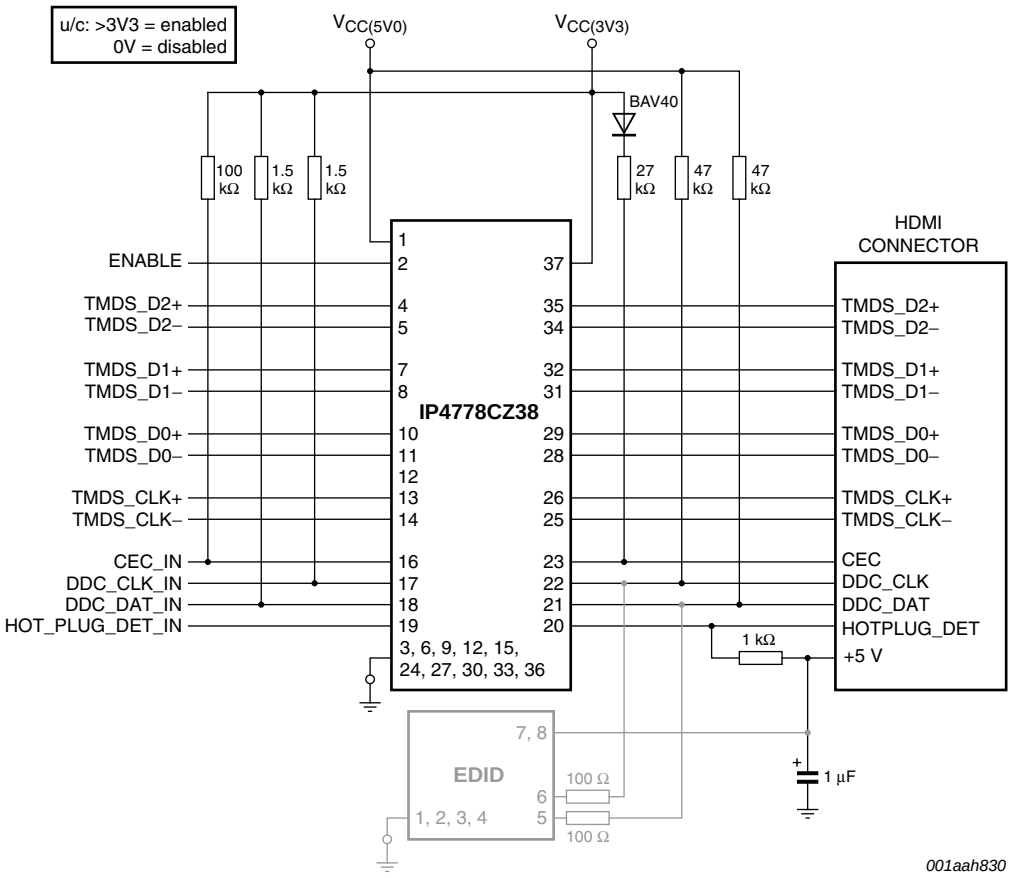



**Fig 14. Schematic of IP4778CZ38 application**

## 10.8 Typical application

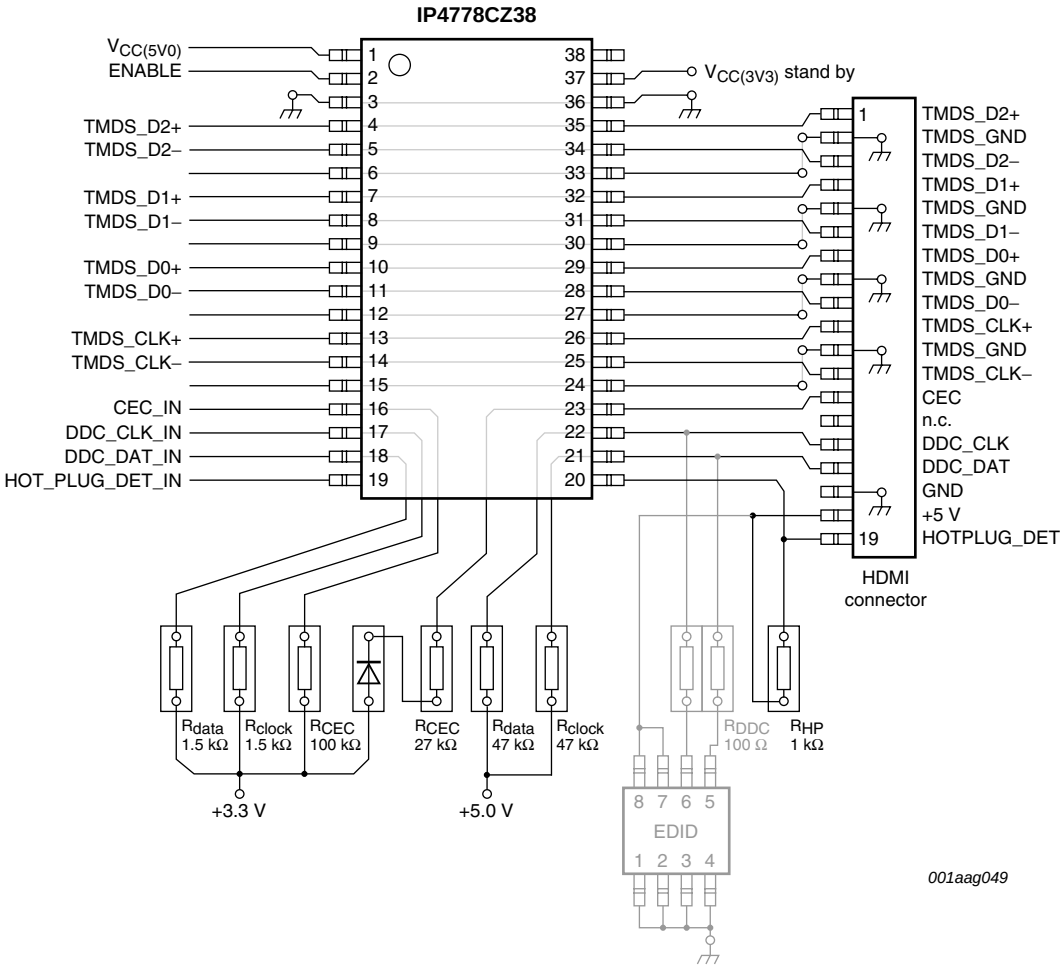


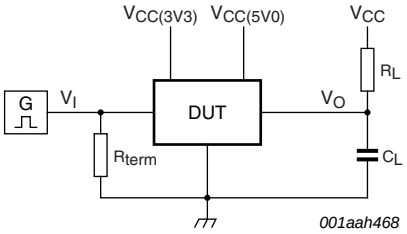

**Fig 15. Application showing optimized PCB microstrip lines**

This application ensures that the EDID (stored in the EEPROM) can be read out in Standby mode, even if long cables are used, to guarantee correct CEC wake-up handling. To wake up the system from Standby to normal operation, the HDMI source has to first read the EDID in order to hand over the port ID via the CEC protocol. This ensures that the HDMI starts up and switches to the correct HDMI port to display the HDMI source which initiates the CEC wake-up sequence.

The CEC bus is enabled by activating the $V_{CC(3V3)}$ standby supply.

The RF routing optimized pin position variant allows optimum design layout of the RF routing microstrips to ensure that the impedance of the TMDS lines remain within the specification limits. Part of the microstrips comprise a solid ground plane which is located beneath the device.

# 11. Test information




See Table 10 for test data.

$R_{term}$ = termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$R_L$ = load resistance.

$C_L$ = load capacitance.

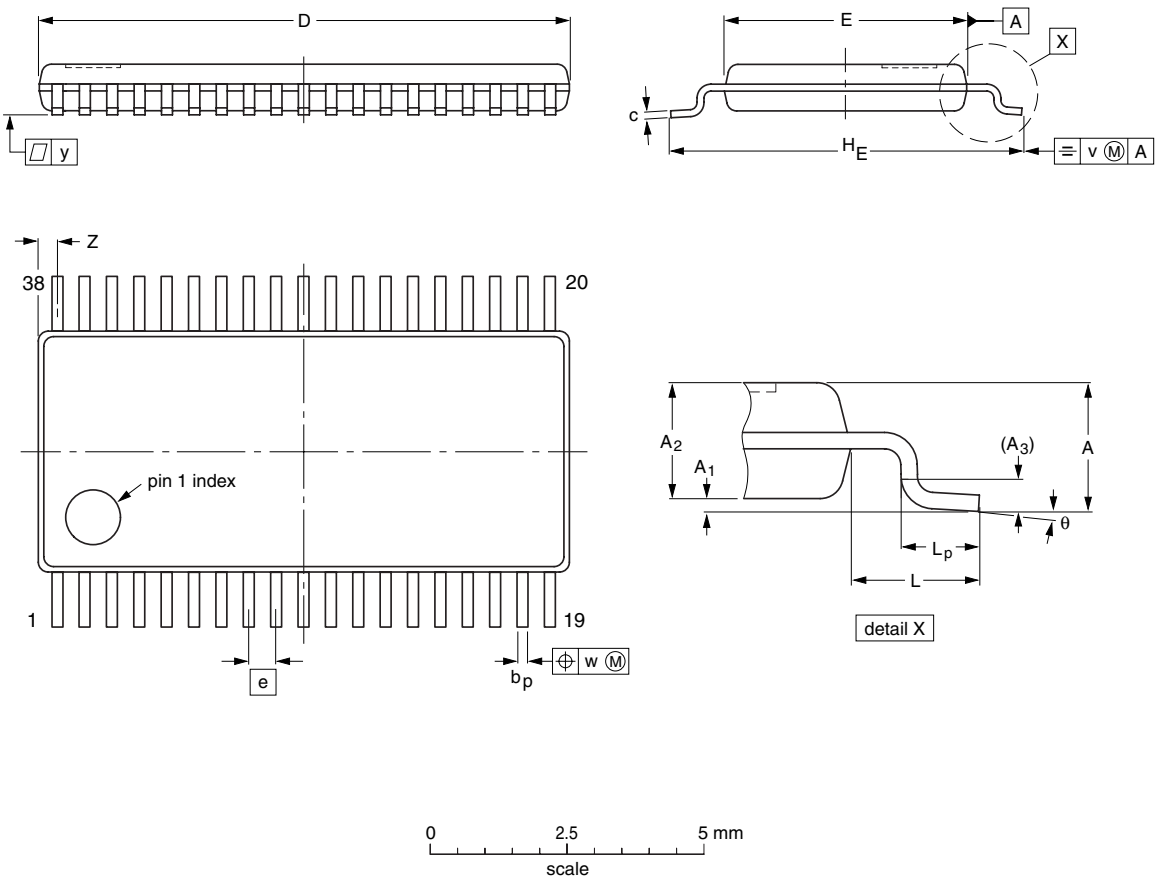
**Fig 16. Test circuit for DDC and CEC lines**

**Table 10. Test data**

| Test | $R_L$ | $C_L$ | $V_{CC}$ |
|---|---|---|---|
| DDC lines | 1.35 kΩ | 50 pF | $V_{CC(5V0)}$ |
| CEC line | 27 kΩ | 50 pF | $V_{CC(3V3)}$ |

## 12. Package outline

**TSSOP38: plastic thin shrink small outline package; 38 leads; body width 4.4 mm; lead pitch 0.5 mm** **SOT510-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1 | 0.15<br>0.05 | 0.95<br>0.85 | 0.25 | 0.27<br>0.17 | 0.20<br>0.09 | 9.8<br>9.6 | 4.5<br>4.3 | 0.5 | 6.4 | 1 | 0.7<br>0.5 | 0.2 | 0.08 | 0.08 | 0.49<br>0.21 | $8^o$<br>$0^o$ |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT510-1 | | MO-153 | | | | ~~03-02-18~~<br>05-11-02 |

**Fig 17. Package outline SOT510-1 (TSSOP38)**

# 13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

## 13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

## 13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

## 13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

## 13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 18) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 11 and 12

**Table 11. SnPb eutectic process (from J-STD-020C)**

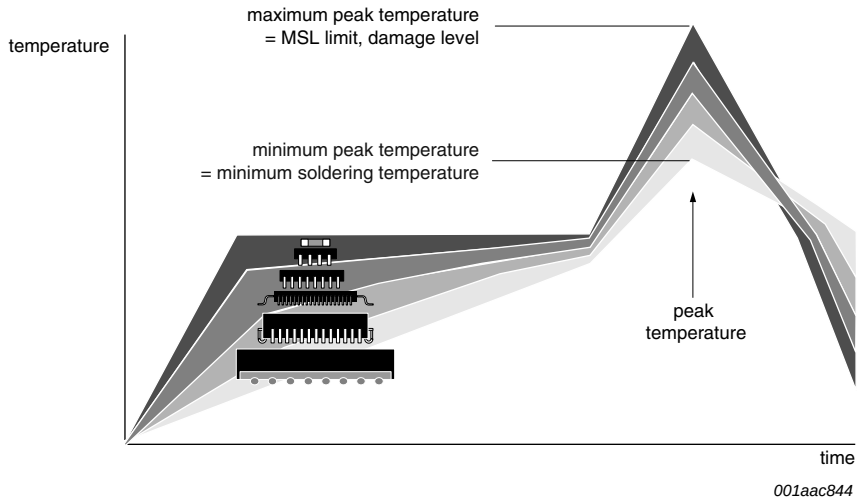
| Package thickness (mm) | Package reflow temperature (°C) | |
|---|---|---|
| | Volume ($mm^3$) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

**Table 12. Lead-free process (from J-STD-020C)**

| Package thickness (mm) | Package reflow temperature (°C) | | |
|---|---|---|---|
| | Volume ($mm^3$) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 18.




MSL: Moisture Sensitivity Level

**Fig 18. Temperature profiles for large and small components**

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

## 14. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| CEC | Consumer Electronics Control |
| DDC | Data Display Channel |
| DVD | Digital Video Disk |
| DVI | Digital Video Interface |
| EDID | Extended Display Identification Data |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| ESD | ElectroStatic Discharge |
| FET | Field-Effect Transistor |
| GPIO | General Purpose Input/Output |
| HDMI | High-Definition Multimedia Interface |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| RoHS | Restriction of Hazardous Substances |
| TMDS | Transition Minimized Differential Signaling |

## 15. Glossary

**HDMI sink —** Device which receives HDMI signals e.g. a TV set.

**HDMI source —** Device which transmit HDMI signal e.g. a DVD player.

# 16. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| IP4778CZ38 v.3 | 20110331 | Product data sheet | - | IP4778CZ38 v.2 |
| Modifications: | • Section 1 “General description”: updated.<br>• Section 2 “Features and benefits”: updated.<br>• Section 14 “Abbreviations”: updated.<br>• Section 17 “Legal information”: updated. | | | |
| IP4778CZ38 v.2 | 20090212 | Product data sheet | - | IP4778CZ38 v.1 |
| IP4778CZ38 v.1 | 20080410 | Objective data sheet | - | - |

# 17. Legal information

## 17.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 17.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 17.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

**Quick reference data —** The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 17.4 Licenses

**Purchase of NXP ICs with HDMI technology**

Use of an NXP IC with HDMI technology in equipment that complies with the HDMI standard requires a license from HDMI Licensing LLC, 1060 E. Arques Avenue Suite 100, Sunnyvale CA 94085, USA, e-mail: admin@hdmi.org.

## 17.5 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

# 18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 19. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 31 March 2011**
**Document identifier: IP4778CZ38**