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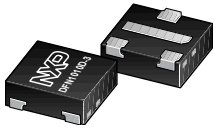
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Kind regards,

Team Nexperia



PMXB75UPE

20 V, P-channel Trench MOSFET

8 July 2014

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1010D-3 (SOT1215) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: 1.1 × 1.0 × 0.37 mm
- Exposed drain pad for excellent thermal conduction
- ElectroStatic Discharge (ESD) protection 1.5 kV HBM
- Drain-source on-state resistance $R_{DS(on)} = 69 \text{ m}\Omega$
- Very low gate-source threshold voltage for portable applications $V_{GS(th)} = -0.68 \text{ V}$

3. Applications

- High-side load switch and charging switch for portable devices
- Power management in battery driven portables
- LED driver
- DC-to-DC converter

4. Quick reference data

Table 1. Quick reference data

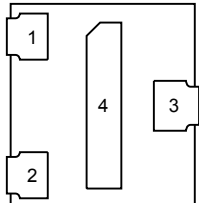
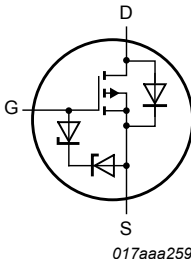
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25 \text{ }^\circ\text{C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$	[1]	-	-2.9	A
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}; I_D = -2.9 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	69	85	$\text{m}\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1010D-3 (SOT1215)</p>	 <p>017aaa259</p>
2	S	source		
3	D	drain		
4	D	drain		

6. Ordering information

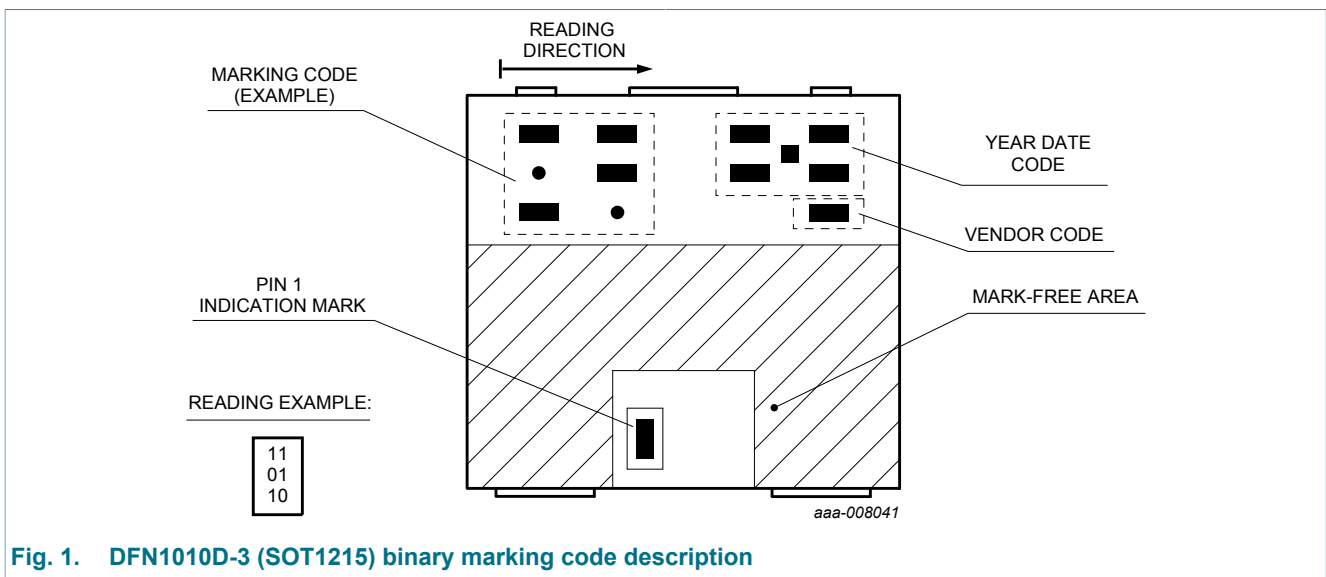
Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PMXB75UPE	DFN1010D-3	DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads; 3 terminals; body 1.1 x 1.0 x 0.37 mm	SOT1215

7. Marking

Table 4. Marking codes

Type number	Marking code
PMXB75UPE	00 01 00



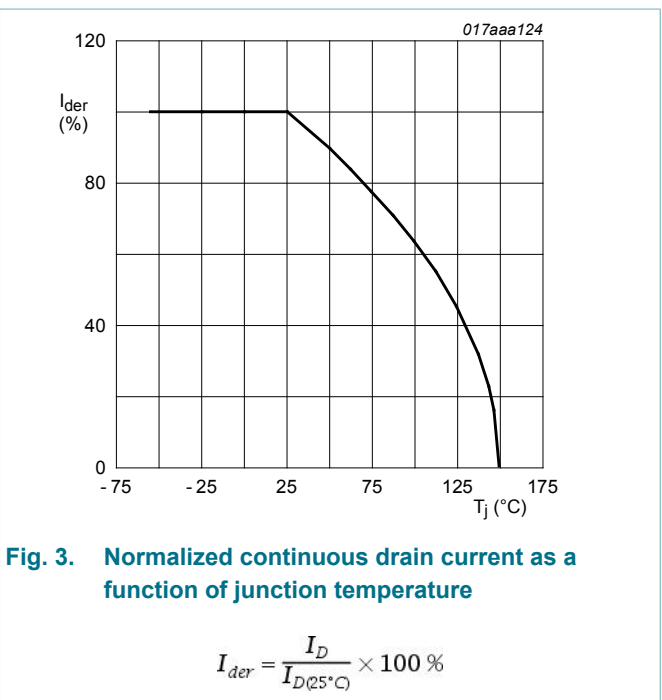
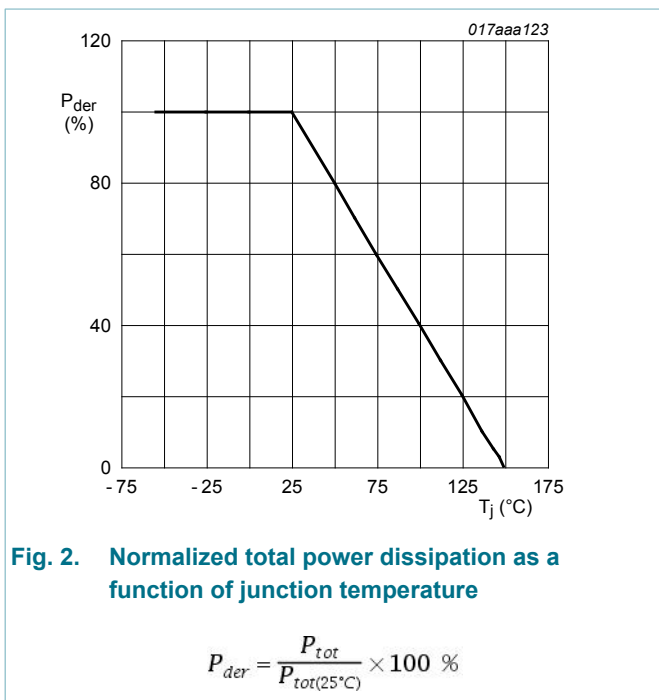
8. Limiting values

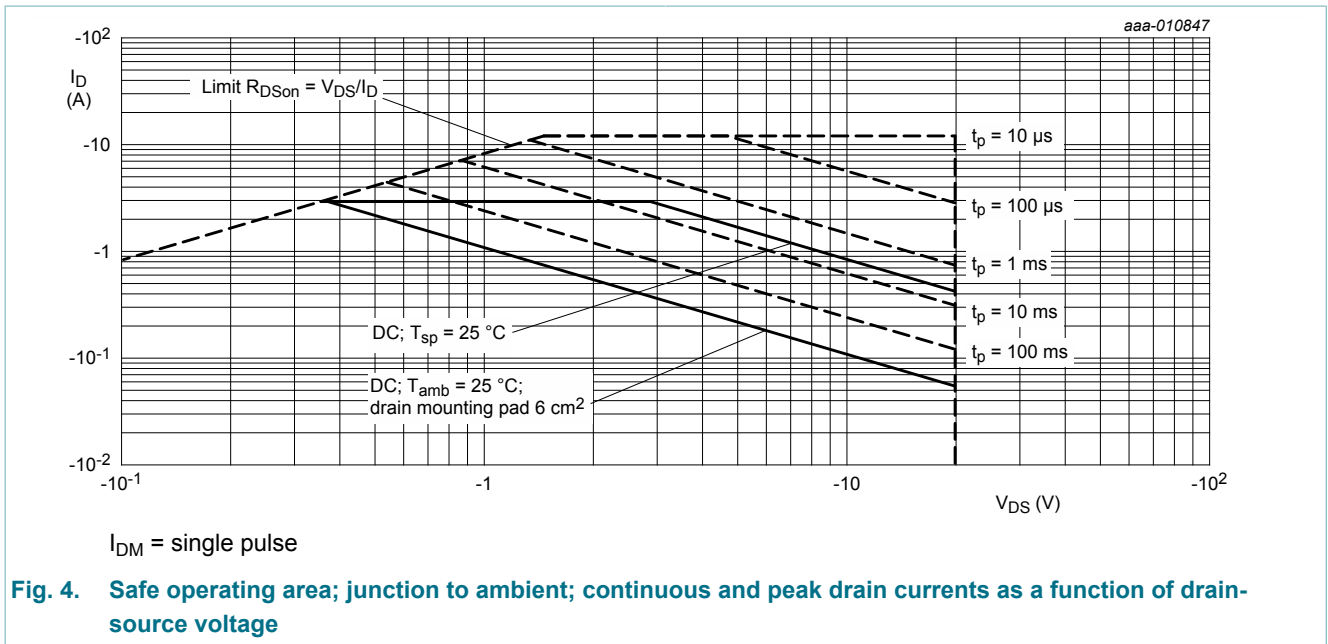
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-2.9	A
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-1.9	A
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-12	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	317	mW
			[1]	-	1070	mW
		T _{sp} = 25 °C		-	8330	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-1	A

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.





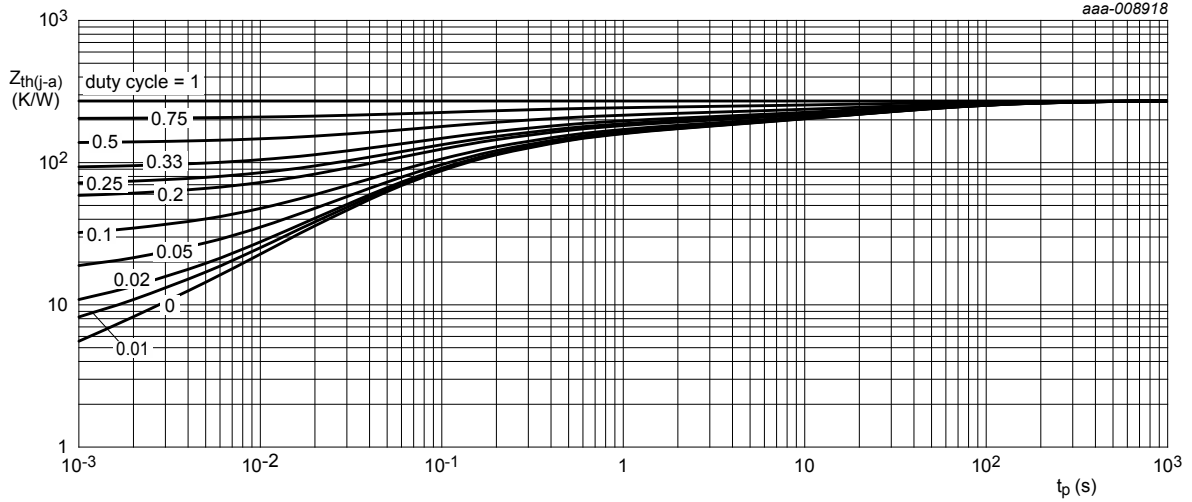
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	271	312	K/W
			[2]	-	102	117	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	10	15	K/W

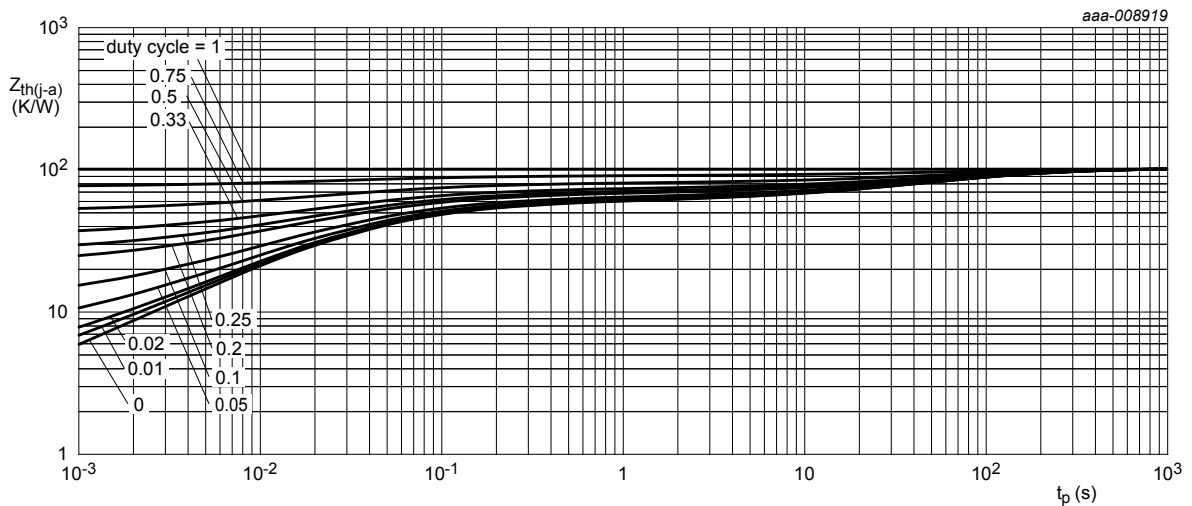
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm^2 .



FR4 PCB, standard footprint

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm^2

Fig. 6. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	-0.4	-0.68	-1	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
I_{GSS}	gate leakage current	$V_{GS} = -8 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 8 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 4.5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V$; $I_D = -2.9 A$; $T_j = 25 \text{ }^\circ C$	-	69	85	m Ω
		$V_{GS} = -4.5 V$; $I_D = -2.9 A$; $T_j = 150 \text{ }^\circ C$	-	99	122	m Ω
		$V_{GS} = -2.5 V$; $I_D = -2.6 A$; $T_j = 25 \text{ }^\circ C$	-	86	110	m Ω
		$V_{GS} = -1.8 V$; $I_D = -0.4 A$; $T_j = 25 \text{ }^\circ C$	-	130	200	m Ω
		$V_{GS} = -1.5 V$; $I_D = -50 \text{ mA}$; $T_j = 25 \text{ }^\circ C$	-	205	450	m Ω
		$V_{GS} = -1.2 V$; $I_D = -10 \text{ mA}$; $T_j = 25 \text{ }^\circ C$	-	950	-	m Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V$; $I_D = -2 A$; $T_j = 25 \text{ }^\circ C$	-	8.4	-	S
R_G	gate resistance	$f = 1 \text{ MHz}$	-	11.3	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V$; $I_D = -2.9 A$; $V_{GS} = -4.5 V$; $T_j = 25 \text{ }^\circ C$	-	6.8	12	nC
Q_{GS}	gate-source charge		-	0.9	-	nC
Q_{GD}	gate-drain charge		-	2.1	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	608	-	pF
C_{oss}	output capacitance		-	75	-	pF
C_{rss}	reverse transfer capacitance		-	64	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V$; $I_D = -2.9 A$; $V_{GS} = -4.5 V$; $R_{G(ext)} = 6 \text{ } \Omega$; $T_j = 25 \text{ }^\circ C$	-	6	-	ns
t_r	rise time		-	19	-	ns
$t_{d(off)}$	turn-off delay time		-	29	-	ns
t_f	fall time		-	15	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -1 A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-0.7	-1.2	V

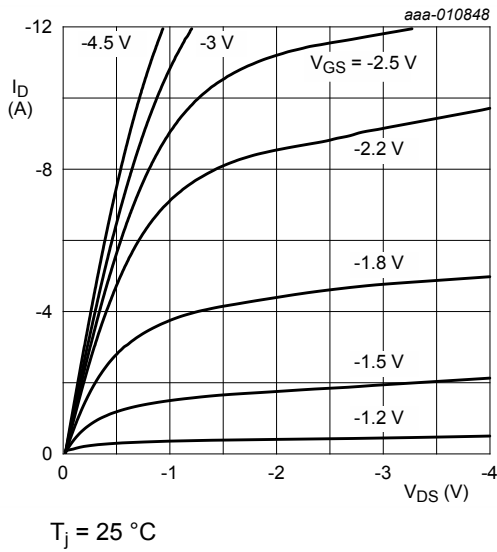


Fig. 7. Output characteristics: drain current as a function of drain-source voltage; typical values

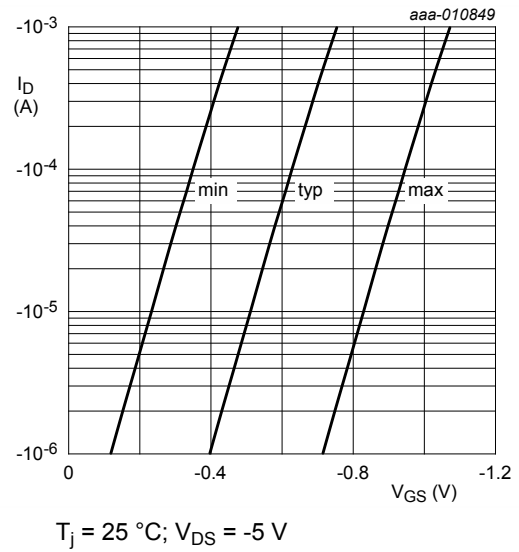


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

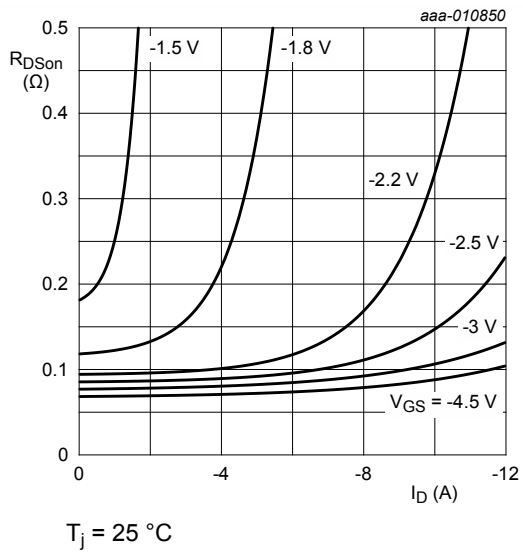


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

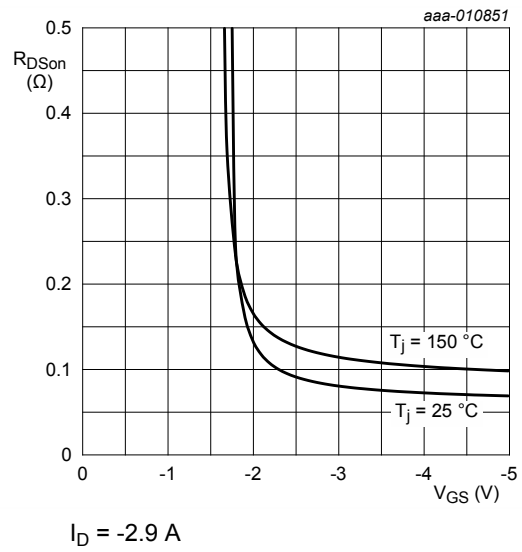


Fig. 10. Drain-source on-state resistance as a function of gate-source voltage; typical values

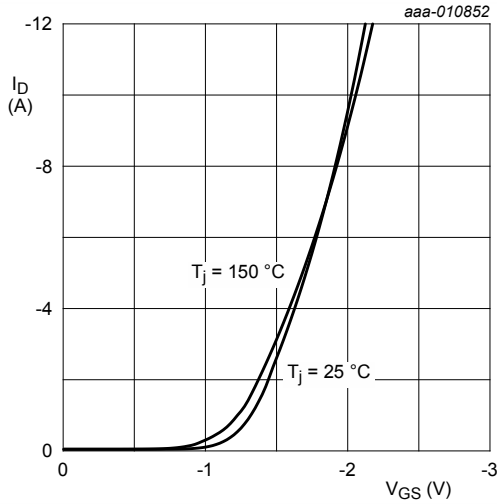


Fig. 11. Transfer characteristics: drain current as a function of gate-source voltage; typical values

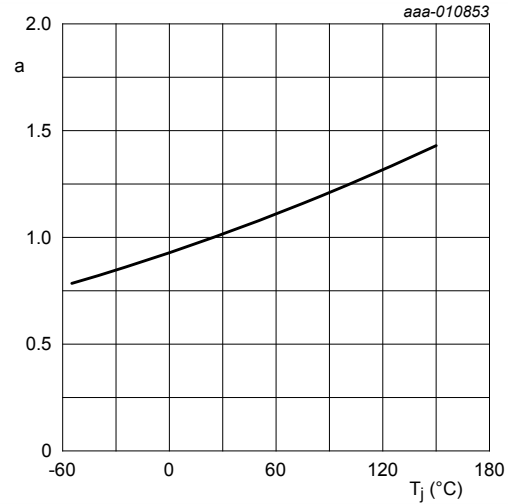


Fig. 12. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}C)}}$$

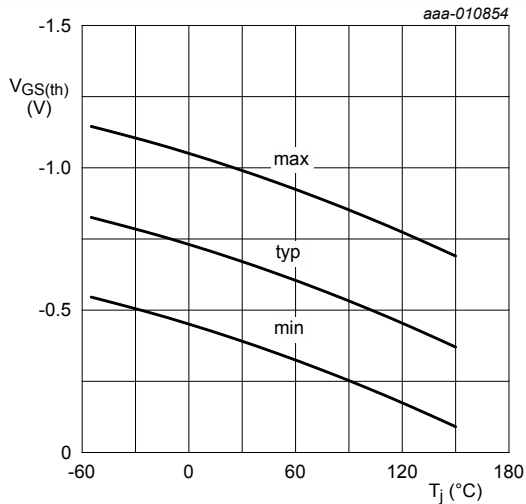


Fig. 13. Gate-source threshold voltage as a function of junction temperature

$I_D = -0.25 \text{ mA}; V_{DS} = V_{GS}$

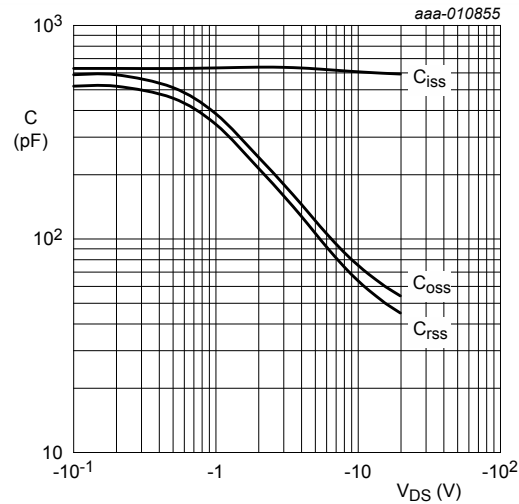
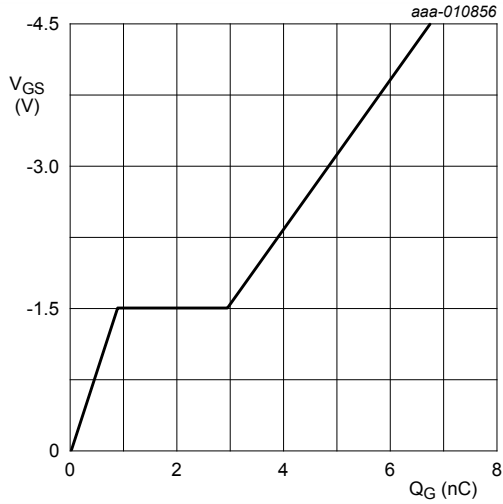


Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$



$I_D = -2.9 \text{ A}; V_{DS} = -10 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

Fig. 15. Gate-source voltage as a function of gate charge; typical values

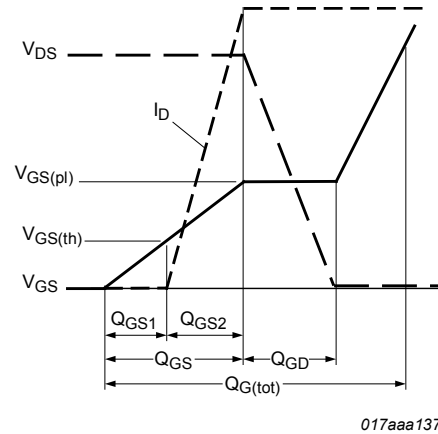
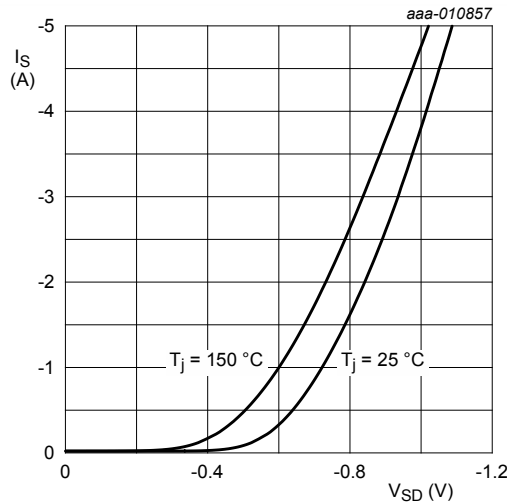


Fig. 16. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 17. Source current as a function of source-drain voltage; typical values

11. Test information

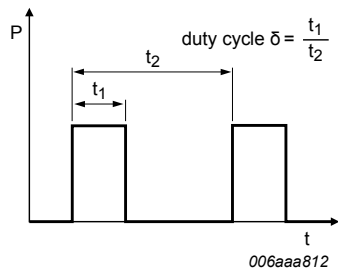
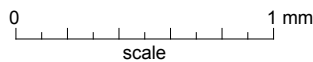
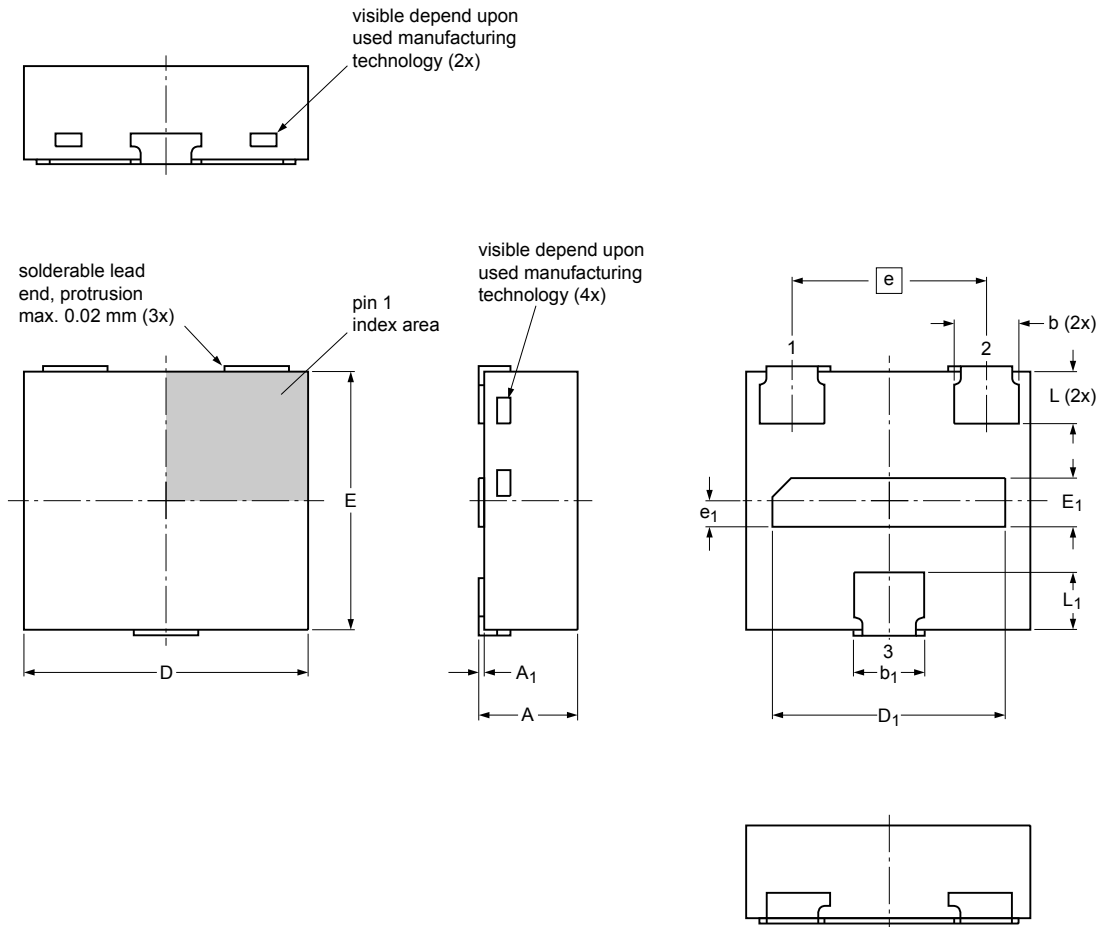


Fig. 18. Duty cycle definition

12. Package outline

DFN1010D-3: plastic thermal enhanced ultra thin small outline package; no leads;
3 terminals; body: 1.1 x 1.0 x 0.37 mm

SOT1215



Dimensions (mm are the original dimensions)

Unit	A	A ₁	b	b ₁	D	D ₁	E	E ₁	e	e ₁	L	L ₁
min	0.34		0.22	0.245	1.05	0.87	0.95	0.16			0.17	0.195
mm nom	0.37		0.25	0.275	1.10	0.90	1.00	0.19	0.75	0.1	0.20	0.225
max	0.40	0.04	0.30	0.325	1.15	0.95	1.05	0.24			0.25	0.275

Note

1. Dimension A is including plating thickness.

sot1215_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1215					-13-03-05- 13-03-06

Fig. 19. Package outline DFN1010D-3 (SOT1215)

13. Soldering

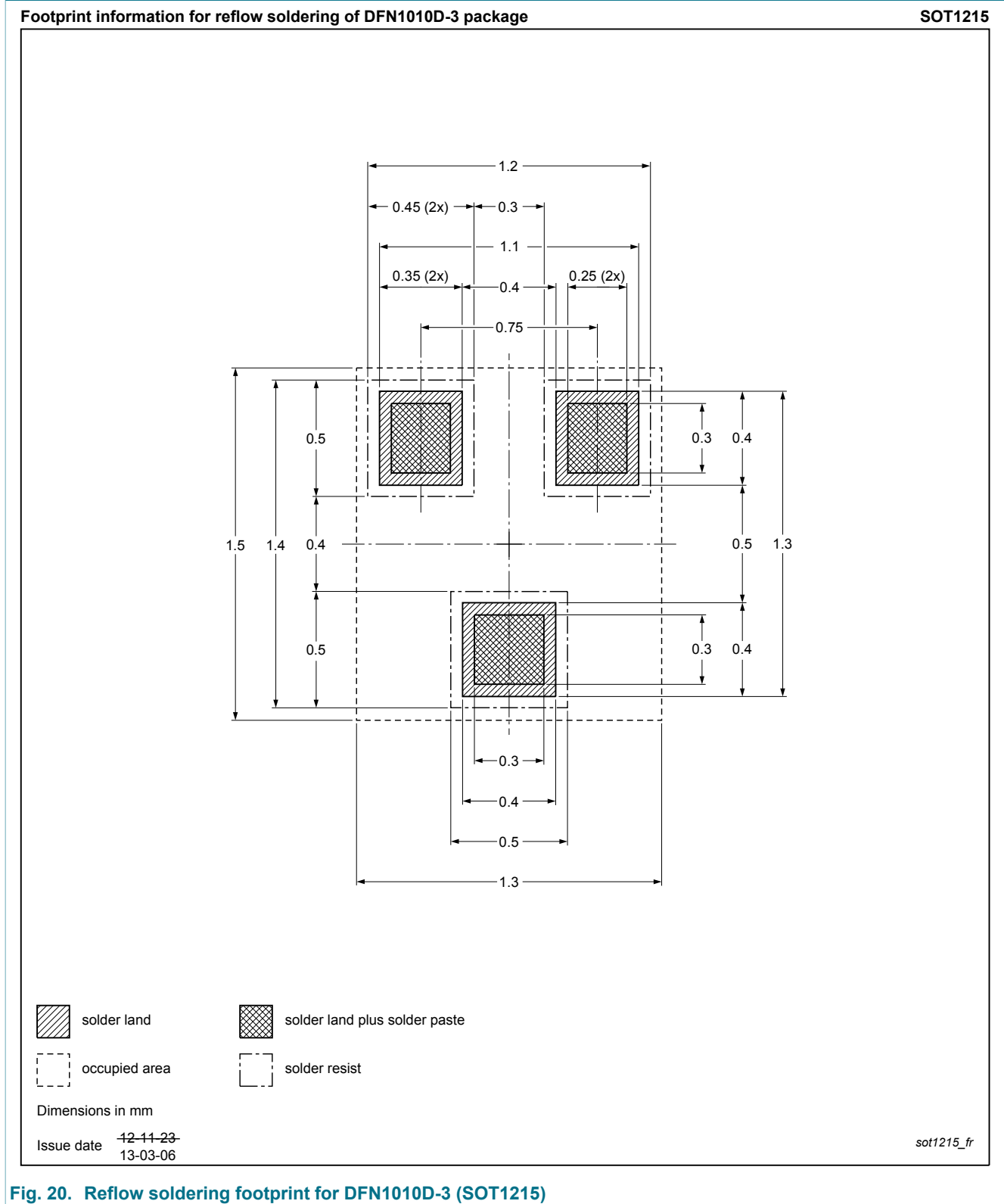


Fig. 20. Reflow soldering footprint for DFN1010D-3 (SOT1215)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMXB75UPE v.3	20140708	Product data sheet	-	PMXB75UPE v.2
Modifications:	<ul style="list-style-type: none">Product status changed			
PMXB75UPE v.2	20140218	Preliminary data sheet	-	PMXB75UPE v.1
PMXB75UPE v.1	20140204	Preliminary data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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