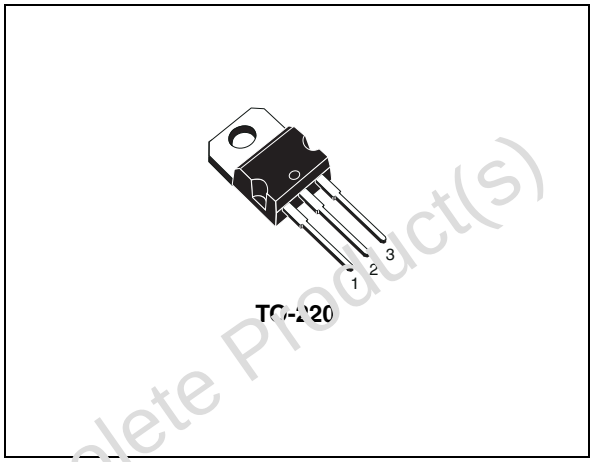
STP5N120

N-channel 1200 V, 2.7 Ω, 4.7 A TO-220 Zener-protected SuperMESH™ Power MOSFET

Features

Type	V_{DSS}	$R_{DS(on)}$	I_D	P_W
STP5N120	1200 V	< 3.5 Ω	4.7 A	160 W

- 100% avalanche tested
- Extremely high dv/dt capability
- ESD improved capability
- New high voltage benchmark
- Gate charge minimized



TO-220

Application

- Switching applications

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage Power MOSFETs.

Figure 1. Internal schematic diagram

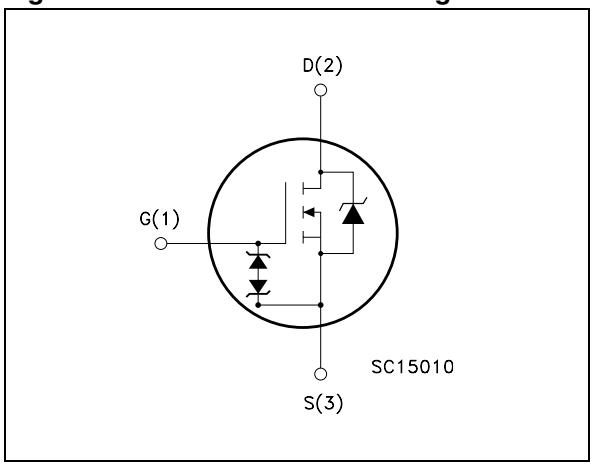


Table 1. Device summary

Order code	Marking	Package	Packaging
STP5N120	5N120	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	1200	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25 °C	4.7	A
I_D	Drain current (continuous) at T_C = 100 °C	3	A
I_{DM} (1)	Drain current (pulsed)	18.8	A
	Derating factor	1.28	W/°C
P_{TOT}	Total dissipation at T_C = 25 °C	160	W
$V_{ESD(G-S)}$	Gate source ESD (HBM-C = 100 pF, R = 1.5 kΩ)	4000	V
dv/dt (2)	Peak diode recovery voltage slope	4	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area
2. I_{SD} ≤ 4.7 A, di/dt ≤ 200 A/µs, V_{DD} ≤ 80% $V_{(BR)DSS}$

Table 3. Thermal data

Symbol	Parameter	Value	Unit
Rthj-case	Thermal resistance junction-case max	0.78	°C/W
Rthj-amb (1)	Thermal resistance junction-amb max	62.5	°C/W
T_l	Maximum lead temperature for soldering purpose	300	°C

1. When mounted on 1inch² FR-4 board, 2 oz Cu

Table 4. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj max)	4.7	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D=I_{AS}, V_{DD}= 50 V)	400	mJ

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1 mA, V_{GS}= 0	1200			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = Max rating, V_{DS} = Max rating,Tc=125 °C			1 50	µA µA
I_{GSS}	Gate body leakage current (V_{DS} = 0)	V_{GS} = ± 20 V			±10	µA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100 µA	3	4	5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10 V, I_D= 2.3 A		2.7	3.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} = 15 V, I_D = 2.3 A		5.8		S
C_{iss}	Input capacitance	V_{DS} =25 V, f=1 MHz, V_{GS}=0	-	2004	-	pF
C_{oss}	Output capacitance			139		pF
C_{rss}	Reverse transfer capacitance			19		pF
$C_{oss\ eq.}$ (2)	Equivalent output capacitance	V_{GS} = 0, V_{DS} = 0 to 960 V	-	89	-	pF
R_G	Intrinsic gate resistance	f = 1MHz open drain	-	2.2	-	Ω
Q_g	Total gate charge	V_{DD} = 960 V, I_D = 4.7 A	-	57	-	nC
Q_{gs}	Gate-source charge	V_{GS} =10 V		10		nC
Q_{gd}	Gate-drain charge	*(see Figure 15)*		31		nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. Coss eq. is defined as a constant equivalent capacitance giving the same charging time as Coss when V_{DS} increases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 600 V, I_D = 2.3 A, R_G=4.7 Ω, V_{GS}=10 V *(see Figure 17)*	-	18	-	ns
t_r	Rise time			9		ns
$t_{d(off)}$	Turn-off delay time			42		ns
t_f	Fall time			30		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain current Source-drain current (pulsed)		-		4.7 18.8	mA A
V_{SD} (1)	Forward on voltage	I_{SD}= 4.7 A, V_{GS}=0	-		1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 4.7 A, V_{DD}= 60 V di/dt = 100 A/µs, *(see Figure 16)*	-	760 5 14		ns µC A
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD}= 4.7 A,V_{DD}= 60 V di/dt=100 A/µs, Tj=150 °C*(see Figure 16)*	-	880 7 160		ns µC A

1. Pulsed: pulse duration = 300µs, duty cycle 1.5%

Table 9. Gate-source Zener diode

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
BV_{GSO}	Gate-source breakdown voltage	Igs ± 1mA, (open drain)	30			V

The built-in-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

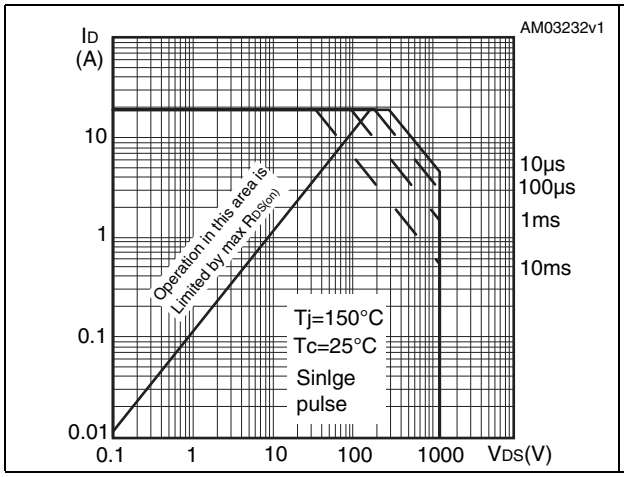


Figure 3. Thermal impedance

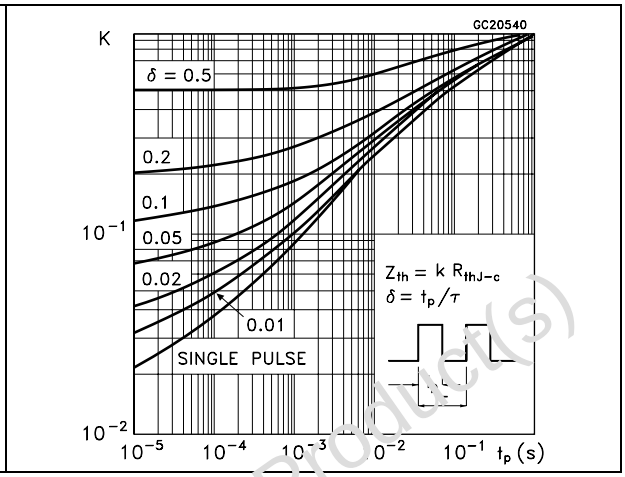


Figure 4. Output characteristics

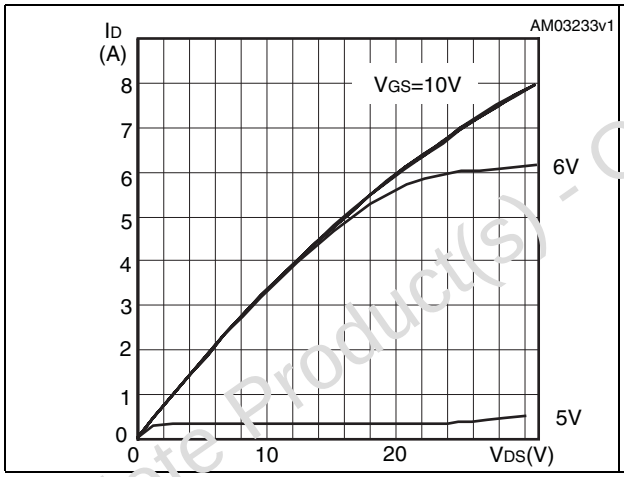


Figure 5. Transfer characteristics

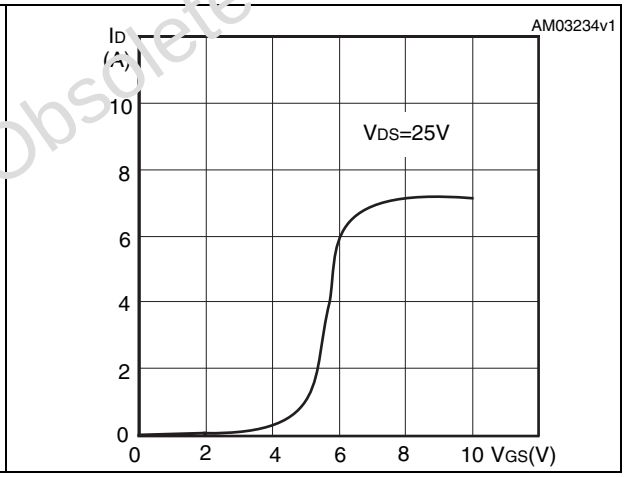


Figure 6. Normalized B_{VDSS} vs temperature

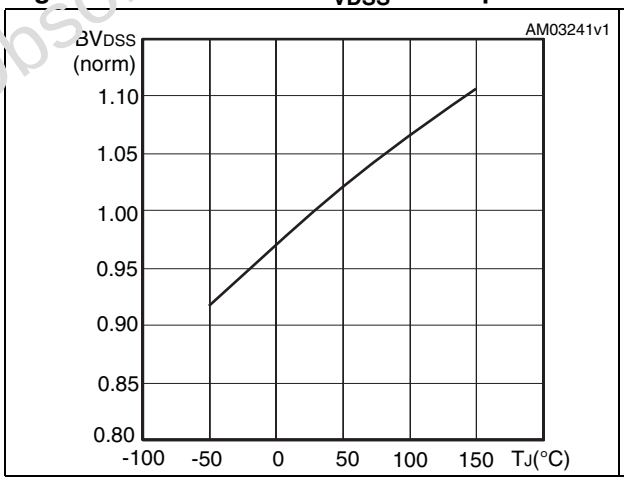


Figure 7. Static drain-source on resistance

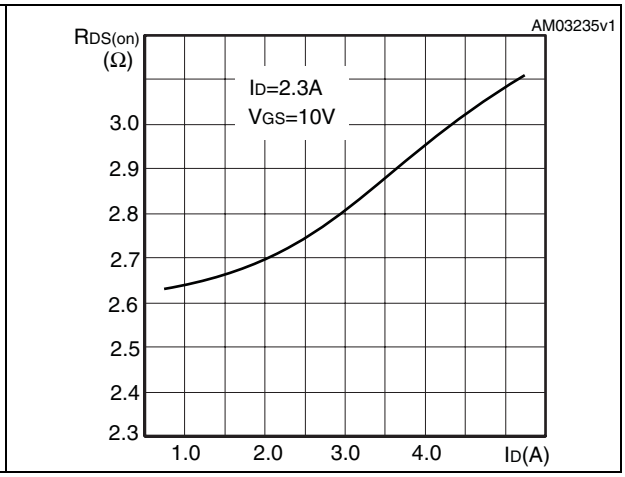


Figure 8. Gate charge vs gate-source voltage

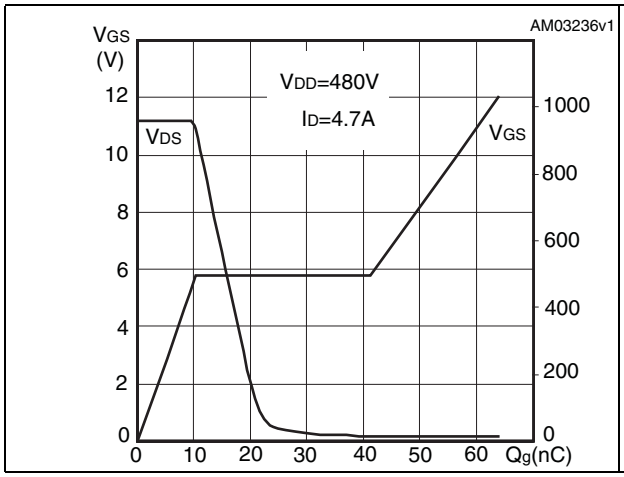


Figure 9. Capacitance variations

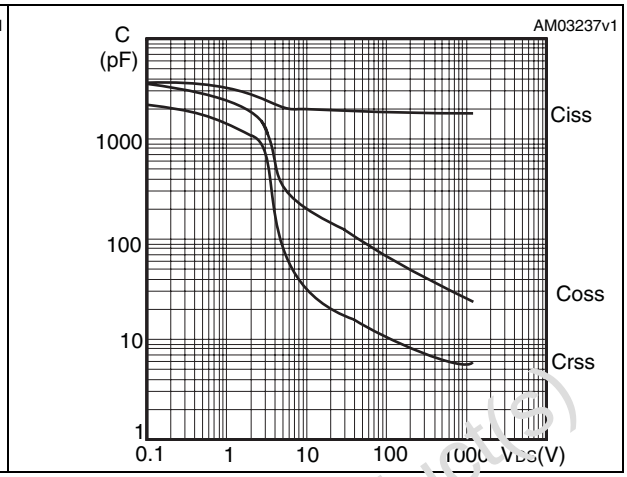


Figure 10. Normalized gate threshold voltage vs temperature

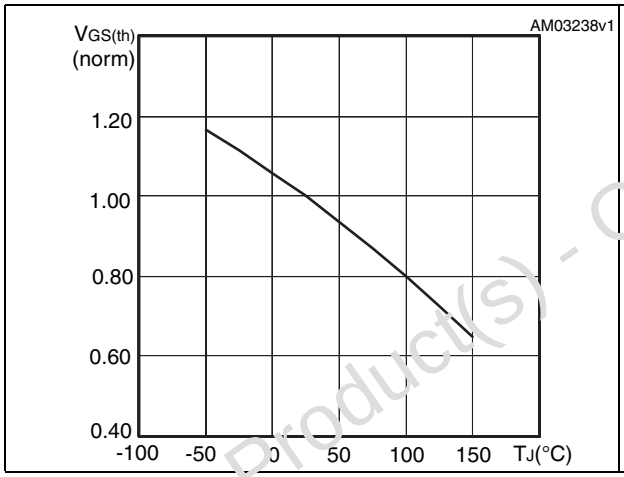


Figure 11. Normalized on resistance vs temperature

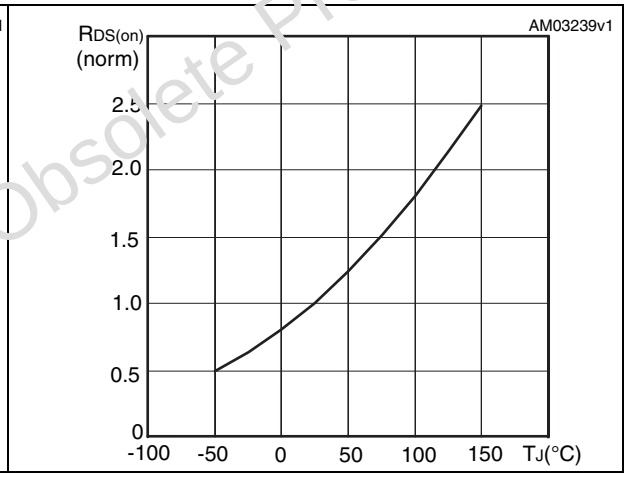


Figure 12. Source-drain diode forward characteristics

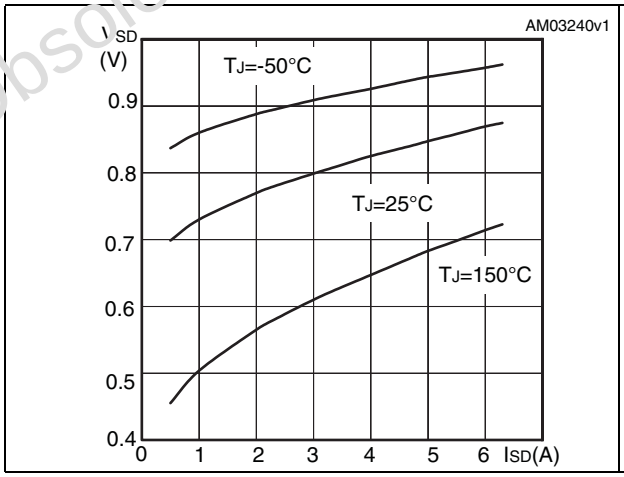
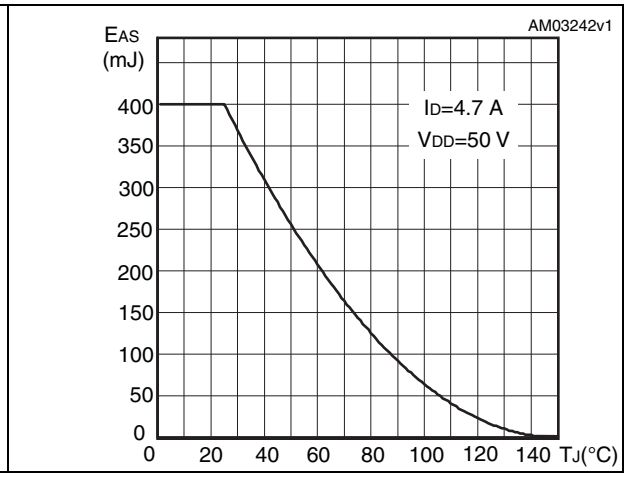


Figure 13. Maximum avalanche energy vs temperature



3 Test circuits

Figure 14. Switching times test circuit for resistive load

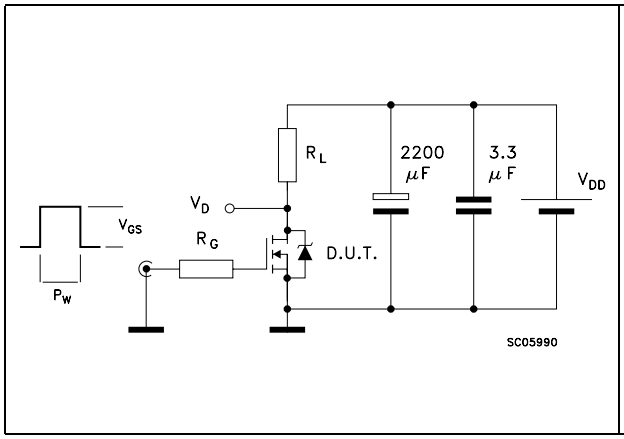


Figure 15. Gate charge test circuit

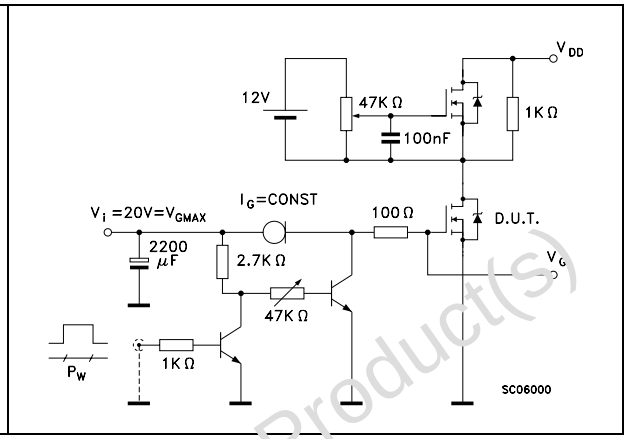


Figure 16. Test circuit for inductive load switching and diode recovery times

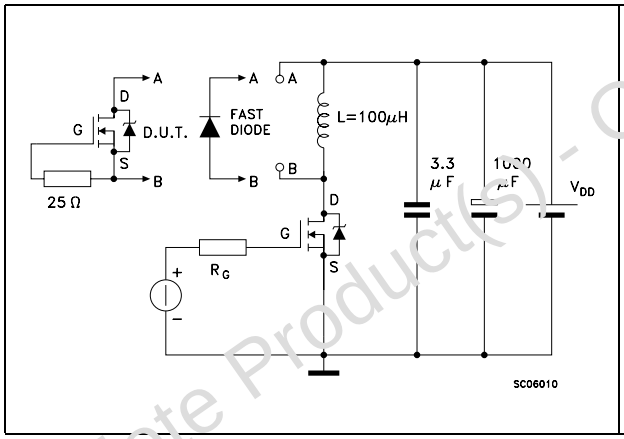


Figure 17. Unclamped inductive load test circuit

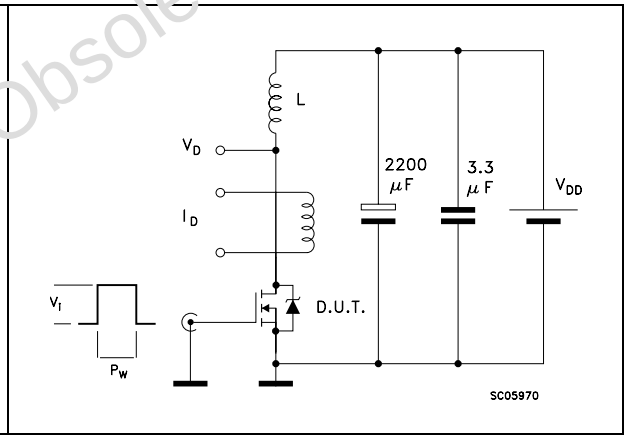


Figure 18. Unclamped inductive waveform

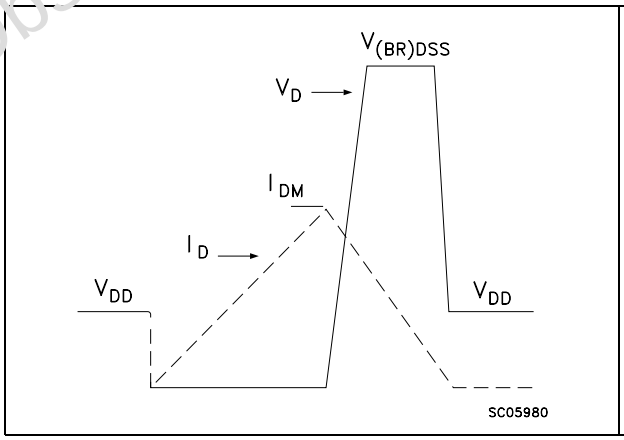
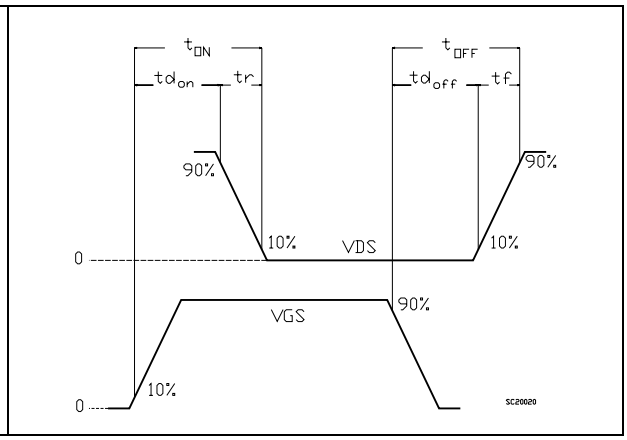


Figure 19. Switching time waveform

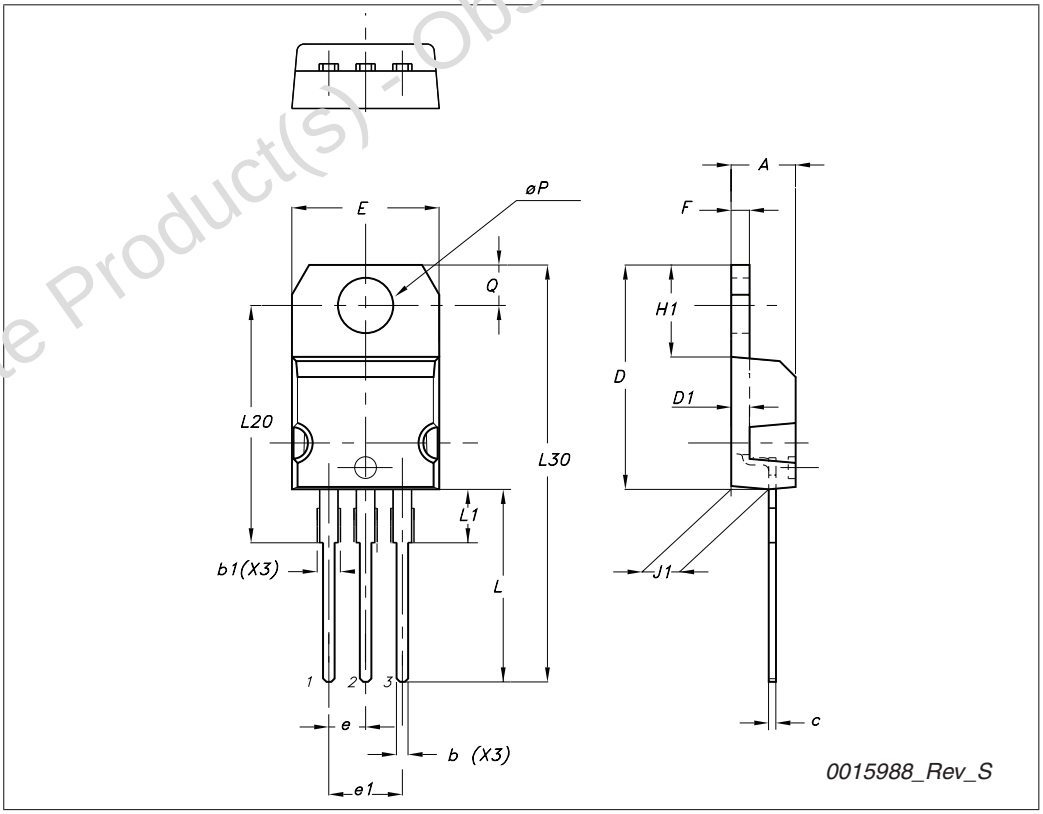


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

TO-220 type A mechanical data

Dim	mm		
	Min	Typ	Max
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
∅P	3.75		3.85
Q	2.65		2.95



5 Revision history

Table 10. Revision history

Date	Revision	Changes
21-May-2007	1	First release
02-Nov-2009	2	Document status promoted from preliminary data to datasheet. Updated mechanical data.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com