INTEGRATED CIRCUITS

DATA SHEET

TDA6120Q
Video output amplifier

Product specification
Supersedes data of 2000 Apr 19
File under Integrated Circuits, IC02

2000 Dec 13

Philips Semiconductors

PHILIPS

Video output amplifier TDA6120Q

FEATURES

- High large-signal bandwidth of 32 MHz (typ.) at 125 V (p-p)
- High small-signal bandwidth of 47 MHz (typ.) at 60 V (p-p)
- Rise/fall time of 12.5 ns for 125 V (p-p)
- High slew rate of 10 V/ns
- Low static power dissipation of 2.6 W at 200 V supply voltage
- High maximum output voltage
- Bandwidth independent of voltage gain
- Maximum overall voltage gain over 46 dB
- High Power Supply Rejection Ratio (PSRR)
- Fast cathode current measurement output for dark current control loop
- Differential voltage input.

GENERAL DESCRIPTION

The TDA6120Q is a single 32 MHz, 125 V (p-p) video output amplifier contained in a plastic DIL-bent-SIL power package. The device uses high-voltage DMOS technology and is intended to drive the cathodes of a CRT in High Definition TVs (HDTVs) or monitors.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA6120Q	DBS13P	plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm)	SOT141-8

BLOCK DIAGRAM

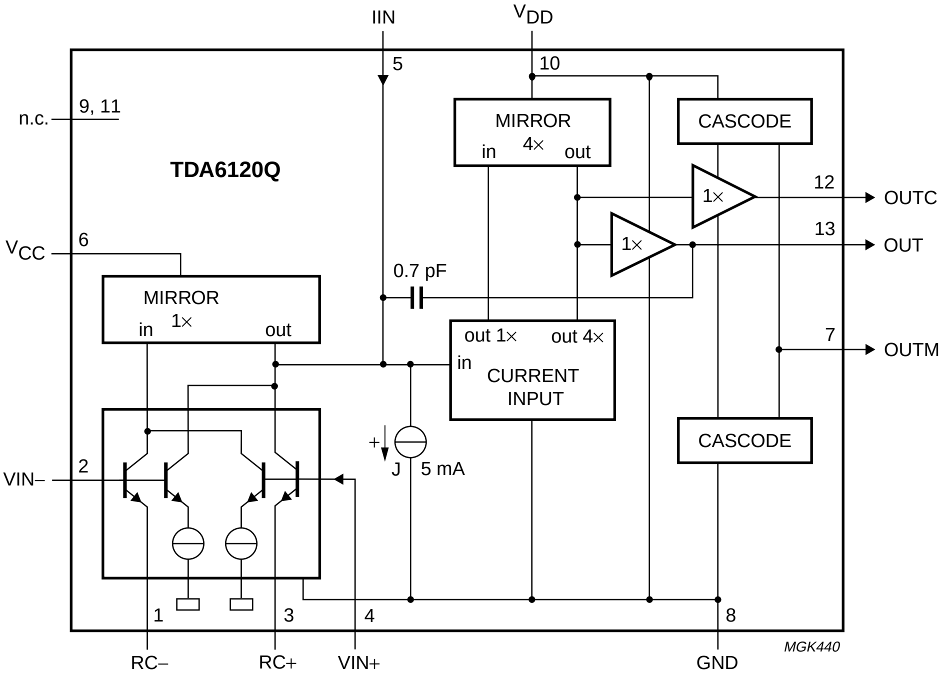


Fig.1 Block diagram.

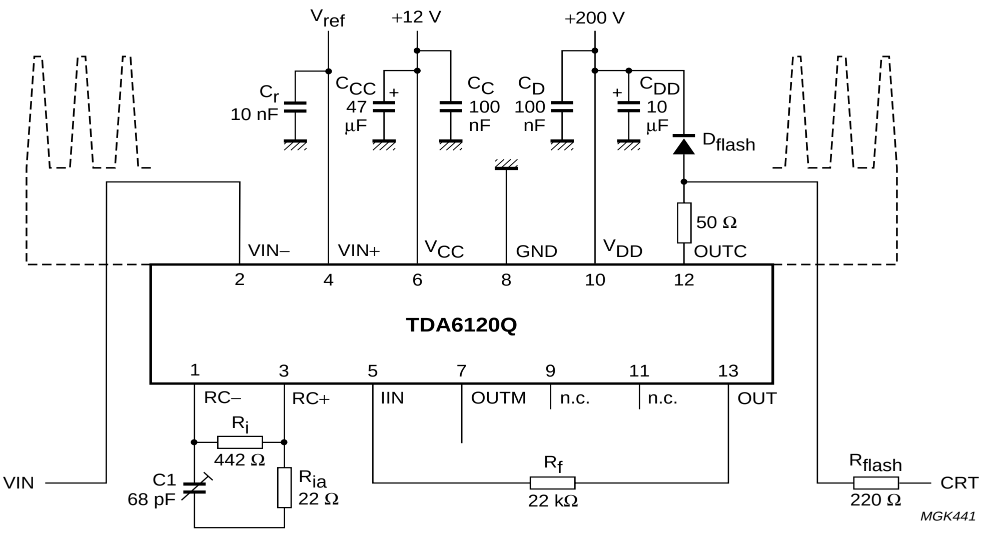


Fig.2 Top view.

PINNING

SYMBOL	PIN	DESCRIPTION
RC–	1	inverting input pre-emphasis network
VIN–	2	inverting voltage input
RC+	3	non-inverting input pre-emphasis network
VIN+	4	non-inverting voltage input
IIN	5	feedback current input
V_{CC}	6	low supply voltage (12 V)
OUTM	7	cathode current measurement output
GND	8	power ground
n.c.	9	not connected
V_{DD}	10	high supply voltage (200 V)
n.c.	11	not connected
OUTC	12	cathode output
OUT	13	feedback output

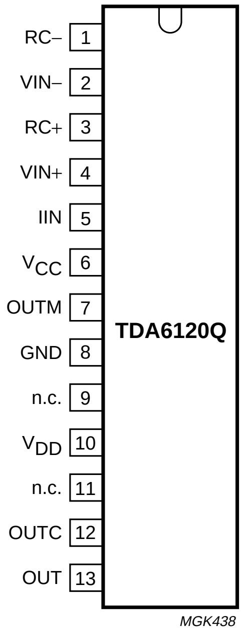
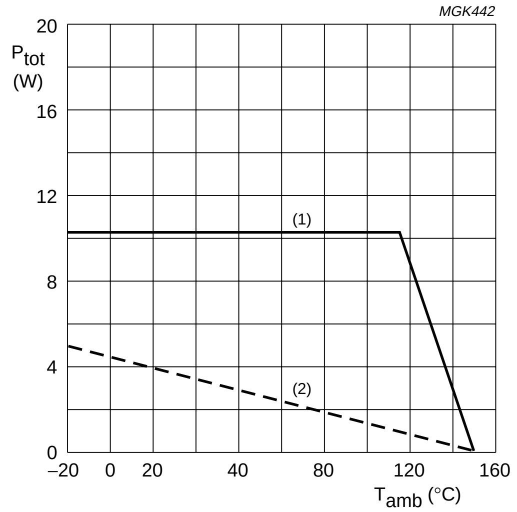


Fig.3 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	high supply voltage	0	280	V
V_{CC}	low supply voltage	0	20	V
V_i	input voltage (pins 2 and 4)	0	V_{CC}	V
$V_{i(dif)}$	differential mode input voltage (pins 2 and 4)	$-V_{CC}$	$+V_{CC}$	V
$V_{i(pe)}$	pre-emphasis input voltage (pins 1 and 3)	0	V_{CC}	V
$V_{i(dif)(pe)}$	differential mode pre-emphasis input voltage (pins 1 and 3)	$-V_{CC}$	$+V_{CC}$	V
V_{IIN}	input voltage (pin 5)	0	$2V_{BE}$	V
V_{OUTM}	measurement output voltage	0	20	V
V_o	output voltage (pins 12 and 13)	0	V_{DD}	V
T_{stg}	storage temperature	–55	+150	°C
T_j	junction temperature	–20	+150	°C
V_{ESD}	voltage peak human body model	–	2000	V
	voltage peak machine model	–	300	V



(1) Infinite heatsink.

(2) No heatsink.

Fig.4 Power derating curve.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th(j-c)}$	thermal resistance from junction to case	3.0	K/W

QUALITY SPECIFICATION

Quality specification in accordance with *“SNW-FQ-611 part D”*.

CHARACTERISTICS

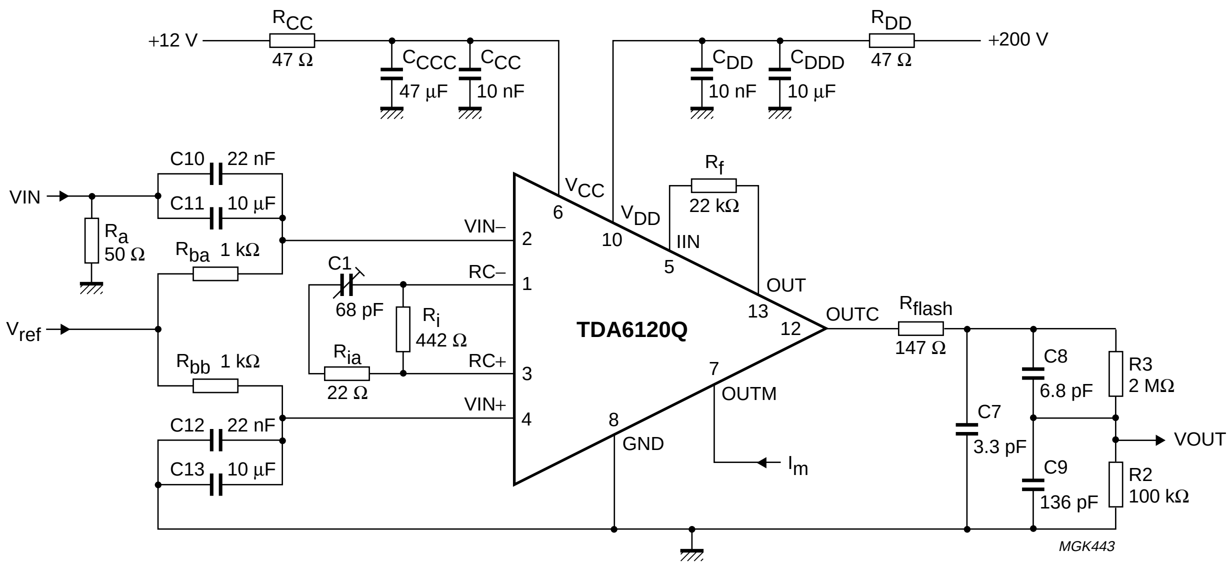
Operating range: T_j = –20 to +150 °C; V_{DD} = 180 to 210 V; V_{CC} = 10.8 to 13.2 V; V_{OUTM} = 3 to 16.5 V; V_{VIN-} = 1.5 to V_{CC} – 6 V; V_{VIN+} = 1.5 to V_{CC} – 6 V. Test conditions: T_j = 25 °C; V_{DD} = 200 V; V_{CC} = 12 V; V_{VIN+} = 3 V; V_{OUTM} = 6 V; C_L = 10 pF (C_L consists of parasitic and cathode capacitance); $R_{th(h-a)}$ = 4 K/W; test circuit of Fig.5; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{DD(q)}$	quiescent high voltage supply current	V_{OUTC} = 100 V	9	11	13	mA
$I_{CC(q)}$	quiescent low voltage supply current	$V_{VIN-} = V_{VIN+}$	35	45	55	mA
I_{bias}	input bias current (pins 2 and 4)	V_{OUTC} = 100 V	–	76	–	μA
V_{OUTC}	DC output voltage (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$	85	103	120	V
$\Delta V_{OUTC(T)}$	DC output voltage temperature drift (pins 12 and 13)	$V_{VIN-} = V_{VIN+}$; temperature range 30 °C < T_j < 110 °C	–100	–25	+55	mV/K
$I_{(offset)OUTM}$	offset current of measurement output	note 1	–30	0	+30	μA
$\Delta I_{OUTM}/\Delta I_{OUTC}$	linearity of current transfer	–50 μA < I_{OUTC} < +50 μA; note 1	–	1.0	–	
C_i	input capacitance (pins 2 and 4)	$V_{OUTC} = V_{OUTC(max)}$	–	4	–	pF
$I_{OUTC(max)}$	maximum dynamic peak output current (pin 12)	20 V < V_{OUTC} < V_{DD} – 20 V	–	100	–	mA
$V_{OUTC(min)}$	minimum output voltage (pin 12)		–	4	10	V
$V_{OUTC(max)}$	maximum output voltage (pin 12)		V_{DD} – 10	V_{DD} – 6	–	V
$V_{CC(sw)}$	V_{CC} switch level at which pins OUT and OUTC become HIGH		–	8.8	–	V
G_{int}	internal gain		1.68	1.87	2.08	
B_s	small-signal bandwidth (pin 12)	$V_{OUTC(AC)}$ = 60 V (p-p); $V_{OUTC(DC)}$ = 100 V	40	47	–	MHz
B_l	large-signal bandwidth (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V	28	32	–	MHz
t_{pd}	cathode output propagation time 50% input to 50% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	10	–	15	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{o(r)}$	cathode output rise time 10% output to 90% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Fig.6	10	12.5	18	ns
$t_{o(f)}$	cathode output fall time 90% output to 10% output (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Fig.7	10	12.5	15	ns
t_{st}	settling time 50% input to (99% < output < 101%) (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	–	350	ns
SR_r	slew rate rise between 30 V to (V_{DD} – 30 V) (pin 12)	V_{VIN-} = 2 V (p-p); square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns	–	8	–	V/ns
SR_f	slew rate fall between (V_{DD} – 30 V) to 30 V (pin 12)	V_{VIN-} = 2 V (p-p); square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns	–	10	–	V/ns
O_{Vr}	cathode output voltage overshoot rise (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	5	–	%
O_{Vf}	cathode output voltage overshoot fall (pin 12)	$V_{OUTC(AC)}$ = 125 V (p-p); $V_{OUTC(DC)}$ = 100 V; square wave; f < 1 MHz; $t_{f(VIN-)}$ = 10 ns; $t_{r(VIN-)}$ = 10 ns; see Figs 6 and 7	–	20	–	%
PSRRh	high voltage power supply rejection ratio	f < 50 kHz; note 2	–	44	–	dB
PSRRl	low voltage power supply rejection ratio	f < 50 kHz; note 2	–	48	–	dB

Notes

1. The operating range of the measurement output OUTM is 3 to 16.5 V. Below 3 V, OUTM acts as a voltage source with an output resistance such that the maximum current input from OUTM is 1.25 mA.
2. The ratio of the change in supply voltage to the change in input voltage when there is no change in output voltage.



$$\text{Overall gain} = G_{int} \times \frac{R_f}{R_i}$$

Fig.5 Test circuit with gain of 40 dB.

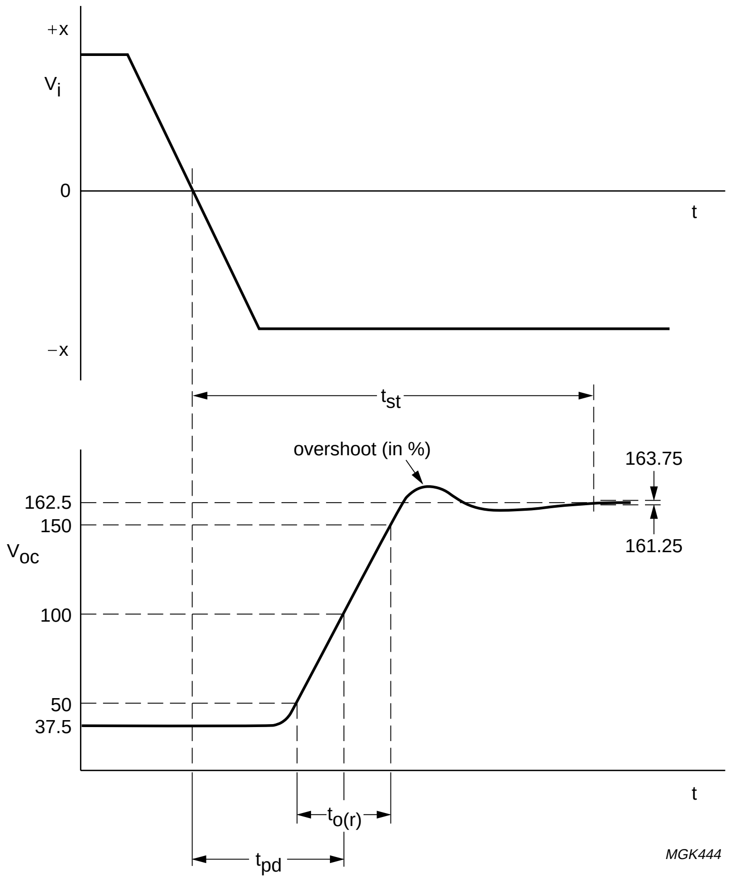


Fig.6 Output (pins 12 and 13; rising edge) as a function of input signal.

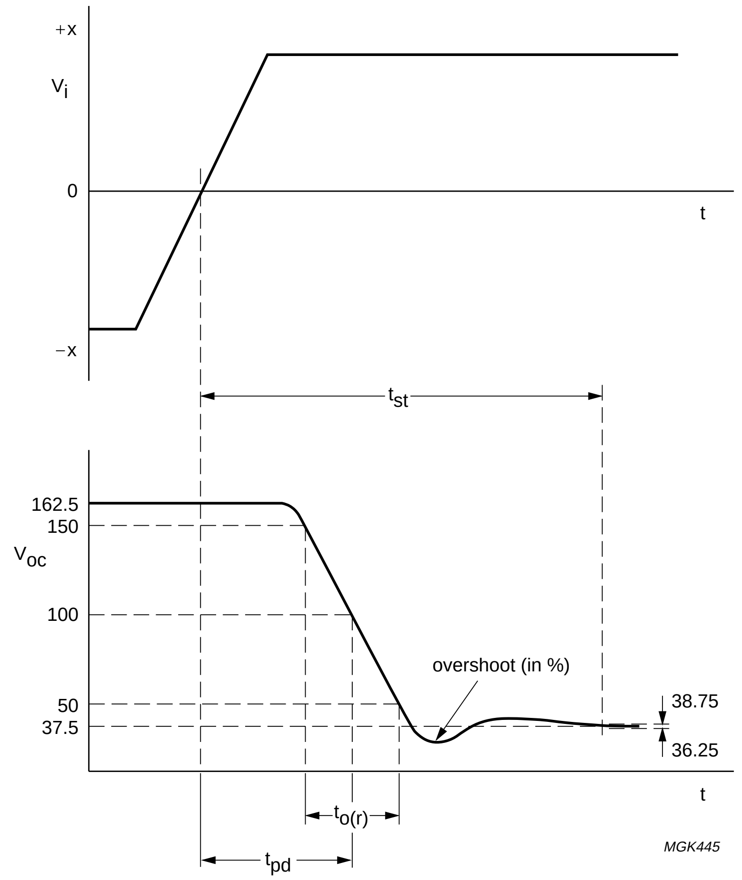


Fig.7 Output (pins 12 and 13; falling edge) as a function of input signal.

FLASHOVER PROTECTION

The TDA6120Q needs an external protection diode combined with a 50 Ω resistor to protect the video amplifier against CRT flashover discharge.

An external 147 Ω carbon high-voltage resistor in combination with a 2 kV spark gap between the cathode and ground will limit the maximum clamp current (for this resistor value, the CRT has to be connected to the main printed-circuit board).

This external network causes an increase in the rise and fall times and a decrease in the overshoot.

Pin 10 must be decoupled to pin 8:

- By a capacitor >100 nF with good HF behaviour (e.g. foil). This capacitor must be placed as close as possible to pins 10 and 8; definitely within 5 mm.
- By a capacitor >10 µF on the picture tube base printed-circuit board (common for 3 output stages).

TEST AND APPLICATION INFORMATION

Dissipation

Regarding dissipation, distinction must be made between static dissipation (independent of frequency) and dynamic dissipation (proportional to frequency). The static dissipation of the TDA6120Q is due to supply currents, and currents in the feedback network and CRT.

The static dissipation is given by the following equation:

$$P_{stat} = V_{CC} \times I_{CC} + V_{DD} \times I_{DD} - V_{OUTC} \times \frac{V_{OUTC}}{R_f} - V_{OUTC} \times I_{OUTC}$$

Where:

R_f = feedback resistance

I_{OUTC} = DC cathode current.

The dynamic dissipation is given by the following equation:
$P_{dyn} = V_{DD} \times (C_L + C_{int}) \times f \times V_{OUTC(p\text{-}p)} \times b$

Where:

C_L = load capacitance

C_{int} = effective internal load capacitance (approximately 7 pF)

f = frequency

$V_{OUTC(p\text{-}p)}$ = output voltage (peak-to-peak value)

b = non-blanking duty cycle (0.8).

The IC must be mounted on the picture tube base printed-circuit board to minimize the load capacitance C_L.

Switch-off

The TDA6120Q is equipped with a switch-off circuit to guarantee a controlled switch-off behaviour of the output pins. The switch-off function is activated when the low supply voltage (V_{CC}) drops below a reference level ($V_{CC(sw)}$). Then the voltage at output pins OUT and OUTC is pulled to the high supply voltage level (V_{DD}), independant of input pin voltage levels.

INTERNAL PIN CONFIGURATION

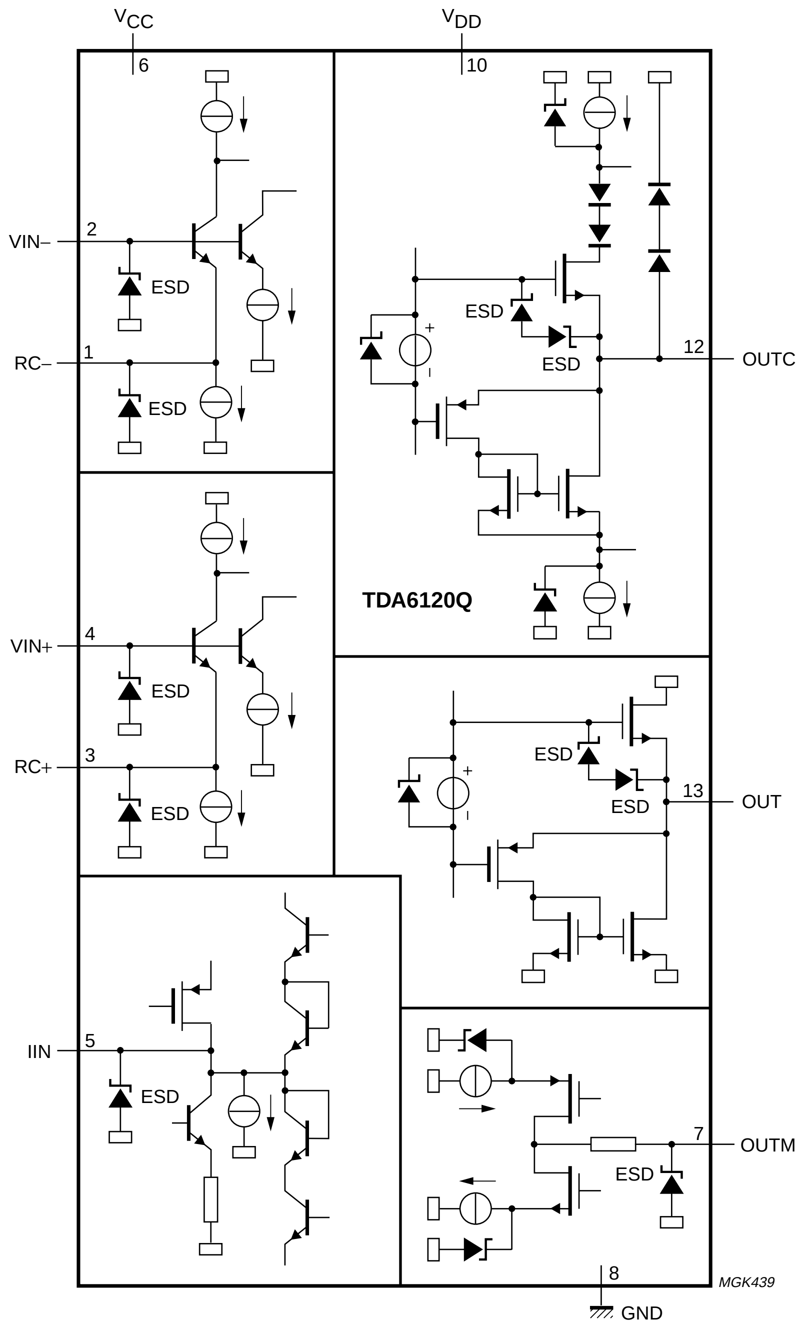
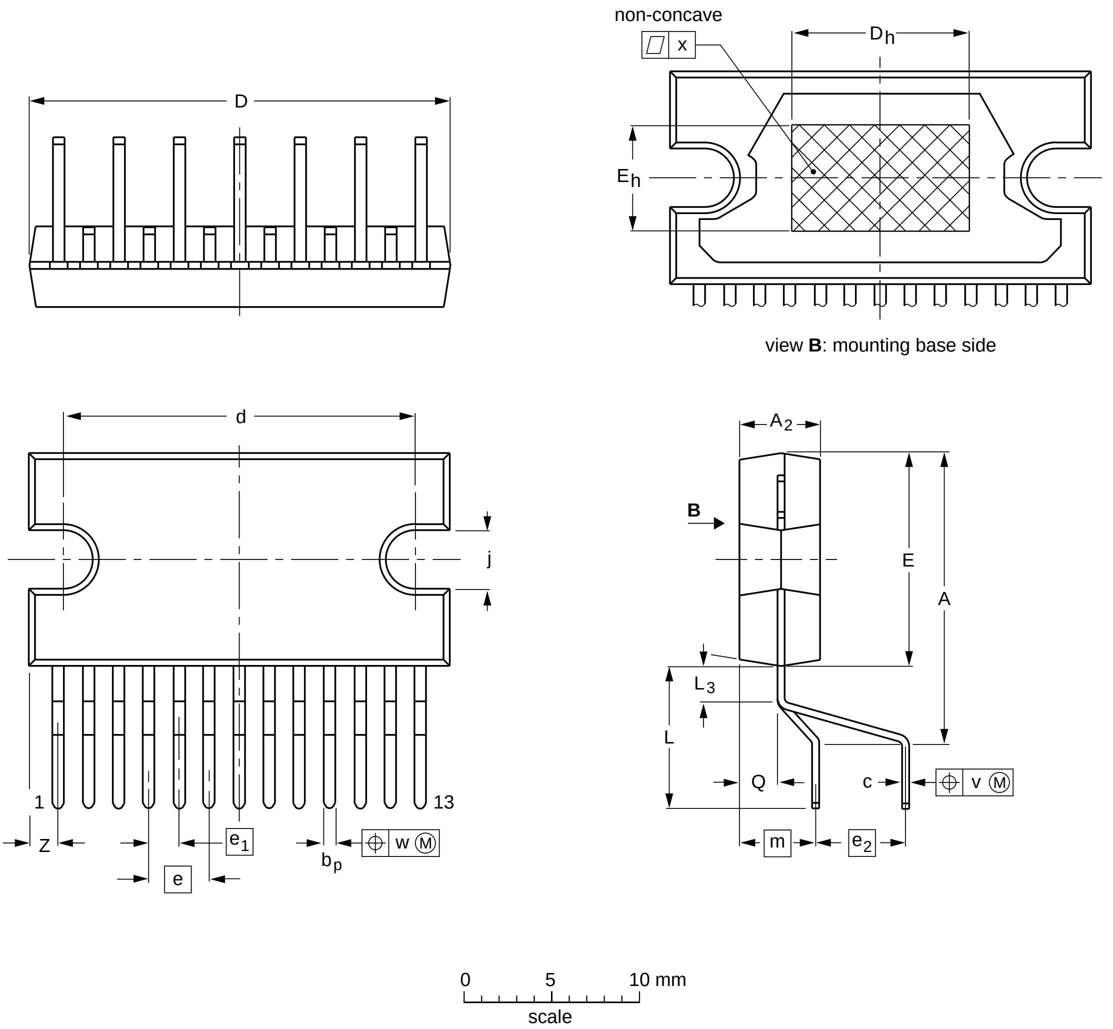


Fig.8 Internal pin diagram.

PACKAGE OUTLINE

DBS13P: plastic DIL-bent-SIL power package; 13 leads (lead length 7.7 mm) **SOT141-8**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_2	b_p	c	$D^{(1)}$	d	D_h	$E^{(1)}$	e	e_1	e_2	E_h	j	L	L_3	m	Q	v	w	x	$Z^{(1)}$
mm	17.0 15.5	4.6 4.4	0.75 0.60	0.48 0.38	24.0 23.6	20.0 19.6	10	12.2 11.8	3.4	1.7	5.08	6	3.4 3.1	8.4 7.0	2.4 1.6	4.3	2.1 1.8	0.6	0.25	0.03	2.00 1.45

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT141-8						~~97-12-16~~ 99-12-17

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable(1)

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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