The following document contains information on Cypress products. Although the document is marked with the name "Spansion" and "Fujitsu", the company that originally developed the specification, Cypress will continue to offer these products to new and existing customers.

Continuity of Specifications
There is no change to this document as a result of offering the device as a Cypress product. Any changes that have been made are the result of normal document improvements and are noted in the document history page, where supported. Future revisions will occur when appropriate, and changes will be noted in a document history page.

Continuity of Ordering Part Numbers
Cypress continues to support existing part numbers. To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information
Please contact your local sales office for additional information about Cypress products and solutions.

About Cypress
Cypress (NASDAQ: CY) delivers high-performance, high-quality solutions at the heart of today's most advanced embedded systems, from automotive, industrial and networking platforms to highly interactive consumer and mobile devices. With a broad, differentiated product portfolio that includes NOR flash memories, F-RAM™ and SRAM, Traveo™ microcontrollers, the industry's only PSoC® programmable system-on-chip solutions, analog and PMIC Power Management ICs, CapSense® capacitive touch-sensing controllers, and Wireless BLE Bluetooth® Low-Energy and USB connectivity solutions, Cypress is committed to providing its customers worldwide with consistent innovation, best-in-class support and exceptional system value.

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13731-5E

16-bit Proprietary Microcontroller
CMOS

F²MC-16LX MB90895 Series

MB90F897/F897S/F897Y*1/F897YS*1/ MB90V495G

■ DESCRIPTION

MB90895 series devices are 16-bit general-purpose microcontrollers designed for applications which need high-speed real-time processing. The devices of this series are high-performance 16-bit CPU microcontrollers employing of the dual operation flash memory and CAN controller on LQFP-48 small package.
The system, inheriting the architecture of F²MC*2 family, employs additional instruction ready for high-level languages, expanded addressing mode, enhanced multiply-divide instructions, and enriched bit-processing instructions. Furthermore, employment of 32-bit accumulator achieves processing of long-word data (32 bits).
The peripheral resources of MB90895 series include the following:
8/10-bit A/D converter, UART0/UART1 (SCI), 8/16-bit PPG timer, 16-bit input-output timer (16-bit free-run timer, input capture 0, 1, 2, 3 (ICU)), and CAN controller.

*1 : These devices are under development. This datasheet provides preliminary information for the devices under development.

*2 : "F²MC" is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Models that support +125°C (MB90F897/S)**
- **Models that support +150°C (MB90F897Y/YS)**
- **Clock**
  - Built-in PLL clock frequency multiplication circuit
  - Selection of machine clocks (PLL clocks) is allowed among frequency division by two on oscillation clock, and multiplication of 1 to 4 times of oscillation clock (for 4-MHz oscillation clock, 4 MHz to 16 MHz).
  - Operation by sub-clock (8.192 kHz) is allowed. (MB90F897/Y)
  - Minimum execution time of instruction: 62.5 ns (when operating with 4-MHz oscillation clock, and 4-time multiplied PLL clock).
- **16 Mbyte CPU memory space**
  - 24-bit internal addressing

(Continued)

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.
http://edevice.fujitsu.com/micom/en-support/

2009.8

(Continued)

- **Instruction system best suited to controller**
  - Wide choice of data types (bit, byte, word, and long word)
  - Wide choice of addressing modes (23 types)
  - Enhanced multiply-divide instructions and RETI instructions
  - Enhanced high-precision computing with 32-bit accumulator
- **Instruction system compatible with high-level language (C language) and multitask**
  - Employing system stack pointer
  - Enhanced various pointer indirect instructions
  - Barrel shift instructions
- **Increased processing speed**
  - 4-byte instruction queue
- **Powerful interrupt function with 8 levels and 34 factors**
- **Automatic data transfer function independent of CPU**
  - Extended intelligent I/O service function (EI^{2}OS): Maximum of 16 channels
- **Low power consumption (standby) mode**
  - Sleep mode (a mode that halts CPU operating clock)
  - Time-base timer mode (a mode that operates oscillation clock, sub clock, time-base timer and watch timer only)
  - Watch mode (a mode that operates sub clock and watch timer only)
  - Stop mode (a mode that stops oscillation clock and sub clock)
  - CPU intermittent operation mode
- **Process**
  - CMOS technology
- **I/O port**
  - General-purpose input/output port (CMOS output) :
    MB90F897/Y : 34 ports (including 4 high-current output ports)
    MB90F897S/YS : 36 ports (including 4 high-current output ports)
- **Timer**
  - Time-base timer, watch timer, watchdog timer: 1 channel
  - 8/16-bit PPG timer: 8-bit x 4 channels, or 16-bit x 2 channels
  - 16-bit reload timer: 2 channels
  - 16-bit input/output timer
    - 16-bit free run timer: 1 channel
    - 16-bit input capture: (ICU): 4 channels

    Interrupt request is issued upon latching a count value of 16-bit free run timer by detection of an edge on pin input.
- **CAN controller: 1 channel**
  - Complied with Ver 2.0A and Ver 2.0B CAN specifications
  - 8 built-in message buffers
  - Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock)
  - CAN wake-up
- **UART0 (SCI), UART1(SCI): 2 channels**
  - Equipped with full-duplex double buffer
  - Clock-asynchronous or clock-synchronous serial transmission is available.
- **DTP/External interrupt: 4 channels, CAN wake-up: 1channel**
  - Module for activation of extended intelligent I/O service (EI^{2}OS), and generation of external interrupt.
- **Delay interrupt generator module**
  - Generates interrupt request for task switching.
- **8/10-bit A/D converter: 8 channels**
  - Resolution is selectable between 8-bit and 10-bit.
  - Activation by external trigger input is allowed.
  - Conversion time: 6.125 µs (at 16-MHz machine clock, including sampling time)
- **Program patch function**
  - Address matching detection for 2 address pointers.

■ PRODUCT LINEUP

Parameter \ Part number		MB90F897 MB90F897S MB90F897Y (Under development) MB90F897YS (Under development)	MB90V495G
Classification		Flash ROM	Evaluation product
ROM capacity		64 Kbytes	—
RAM capacity		2 Kbytes	6 Kbytes
Process		CMOS	
Package		LQFP-48 (pin pitch 0.50 mm)	PGA256
Operating power supply voltage		3.5 V to 5.5 V	4.5 V to 5.5 V
Special power supply for emulator*1		—	None
CPU functions		Number of basic instructions : 351 instructions Instruction length : 1 byte to 7 bytes Data bit length : 1 bit, 8 bits, 16 bits	
		Minimum instruction execution time : 62.5 ns (at 16-MHz machine clock)	
		Interrupt processing time : 1.5 µs at minimum (at 16-MHz machine clock)	
Low power consumption (standby) mode		Sleep mode/Watch mode/Time-base timer mode/ Stop mode/CPU intermittent	
I/O port		General-purpose input/output ports (CMOS output) : 34 ports (36 ports*2) including 4 high-current output ports (P14 to P17)	
Time-base timer		18-bit free-run counter Interrupt cycle : 1.024 ms, 4.096 ms, 16.834 ms, 131.072 ms (with oscillation clock frequency at 4 MHz)	
Watchdog timer		Reset generation cycle: 3.58 ms, 14.33 ms, 57.23 ms, 458.75 ms (with oscillation clock frequency at 4 MHz)	
16-bit input/output timer	16-bit free-run timer	Number of channels: 1 Interrupt upon occurrence of overflow	
	Input capture	Number of channels: 4 Retaining free-run timer value set by pin input (rising edge, falling edge, and both edges)	
16-bit reload timer		Number of channels: 2 16-bit reload timer operation Count clock cycle: 0.25 µs, 0.5 µs, 2.0 µs (at 16-MHz machine clock frequency) External event count is allowed.	
Watch timer		15-bit free-run counter Interrupt cycle: 31.25 ms, 62.5 ms, 12 ms, 250 ms, 500 ms, 1.0 s, 2.0 s (with 8.192 kHz sub clock)	
8/16-bit PPG timer		Number of channels: 2 (four 8-bit channels are available also.) PPG operation is allowed with four 8-bit channels or one 16-bit channel. Outputting pulse wave of arbitrary cycle or arbitrary duty is allowed. Count clock: 62.5 ns to 1 µs (with 16 MHz machine clock)	
Delay interrupt generator module		Interrupt generator module for task switching. Used for real-time OS.	

(Continued)

(Continued)

Part number / Parameter	MB90F897 MB90F897S MB90F897Y (Under development) MB90F897YS (Under development)	MB90V495G
DTP/External interrupt	Number of inputs: 4 Activated by rising edge, falling edge, “H” level or “L” level input. External interrupt or extended intelligent I/O service (EI^{2}OS) is available.	
8/10-bit A/D converter	Number of channels: 8 Resolution: Selectable 10-bit or 8-bit. Conversion time: 6.125 µs (at 16-MHz machine clock, including sampling time) Sequential conversion of two or more successive channels is allowed. (Setting a maximum of 8 channels is allowed.) Single conversion mode : Selected channel is converted only once. Sequential conversion mode: Selected channel is converted repetitively. Halt conversion mode : Conversion of selected channel is stopped and activated alternately.	
UART0 (SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 1,202 bps to 62,500 bps Communication is allowed by bi-directional serial communication function and master/slave type connection.	
UART1 (SCI)	Number of channels: 1 Clock-synchronous transfer: 62.5 kbps to 2 Mbps Clock-asynchronous transfer: 9,615 bps to 500 kbps Communication is allowed by bi-directional serial communication function and master/slave type connection.	
CAN	Complied with Ver 2.0A and Ver 2.0B CAN specifications. 8 built-in message buffers. Transmission rate of 10 kbps to 1 Mbps (by 16 MHz machine clock) CAN wake-up	

*1 : Settings of DIP switch S2 for using emulation pod MB2145-507. For details, see MB2145-507 Hardware Manual (2.7 Power Pin solely for Emulator).

*2 : MB90F897S/YS

■ PACKAGES AND PRODUCT MODELS

Package	MB90F897/S/Y/YS
FPT-48P-M26	○

○ : Yes, × : No

Note : Refer to “■ PACKAGE DIMENSION” for details of the package.

■ PRODUCT COMPARISON

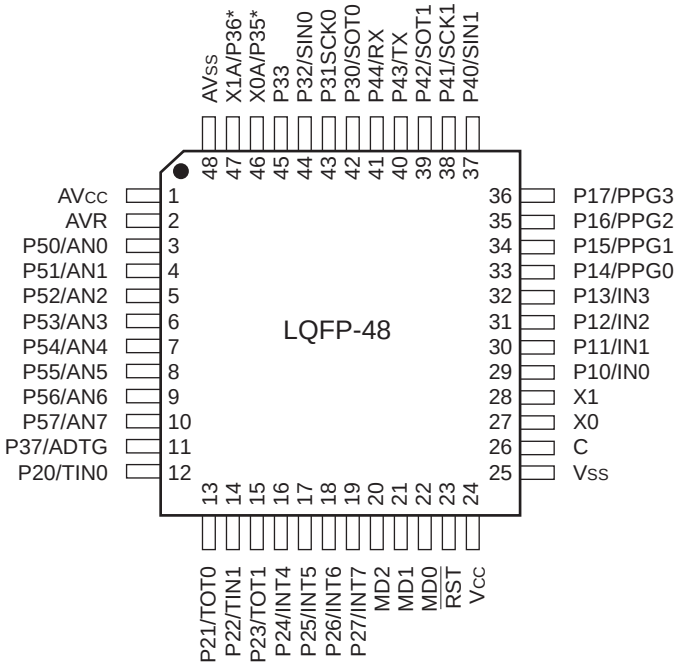
Memory space

When testing with test product for evaluation, check the differences between the product and a product to be used actually. Pay attention to the following points:

- The MB90V495G has no built-in ROM. However, a special-purpose development tool allows the operations as those of one with built-in ROM. ROM capacity depends on settings on a development tool.
- On MB90V495G, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FE0000_H$ to $FF3FFF_H$ is viewed only on FE bank and FF bank. (Modified on settings of a development tool.)
- On MB90F897/S/Y/YS, an image from $FF4000_H$ to $FFFFFF_H$ is viewed on 00 bank and an image of $FF0000_H$ to $FF3FFF_H$ is viewed only on FF bank.

■ PIN ASSIGNMENT

(TOP VIEW)



(FPT-48P-M26)

*: MB90F897/Y : X1A, X0A
MB90F897S/YS : P36, P35

■ PIN DESCRIPTION

Pin No.	Pin name	Circuit type	Function
1	AVcc	—	Vcc power input pin for A/D converter.
2	AVR	—	Power (Vref+) input pin for A/D converter. Use as input for Vcc or lower.
3 to 10	P50 to P57	E	General-purpose input/output ports.
	AN0 to AN7		Functions as analog input pin for A/D converter. Valid when analog input setting is “enabled.”
11	P37	D	General-purpose input/output ports.
	ADTG		Function as an external trigger input pin for A/D converter. Use the pin by setting as input port.
12	P20	D	General-purpose input/output ports.
	TIN0		Function as an event input pin for reload timer 0. Use the pin by setting as input port.
13	P21	D	General-purpose input/output ports.
	TOT0		Function as an event output pin for reload timer 0. Valid only when output setting is “enabled.”
14	P22	D	General-purpose input/output ports.
	TIN1		Function as an event input pin for reload timer 1. Use the pin by setting as input port.
15	P23	D	General-purpose input/output ports.
	TOT1		Function as an event output pin for reload timer 1. Valid only when output setting is “enabled.”
16 to 19	P24 to P27	D	General-purpose input/output ports.
	INT4 to INT7		Functions as external interrupt input pin. Use the pin by setting as input port.
20	MD2	F	Input pin for specifying operation mode. Connect directly to Vss.
21	MD1	C	Input pin for specifying operation mode. Connect directly to Vcc.
22	MD0	C	Input pin for specifying operation mode. Connect directly to Vcc.
23	$\overline{\text{RST}}$	B	External reset input pin.
24	Vcc	—	Power supply (5 V) input pin.
25	Vss	—	Power supply (0 V) input pin.
26	C	—	Capacitor pin for stabilizing power supply. Connect a ceramic capacitor of approximately 0.1 μF.
27	X0	A	Pin for high-rate oscillation.
28	X1	A	Pin for high-rate oscillation.
29 to 32	P10 to P13	D	General-purpose input/output ports.
	IN0 to IN3		Functions as trigger input pins of input capture channels 0 to 3. Use the pins by setting as input ports.

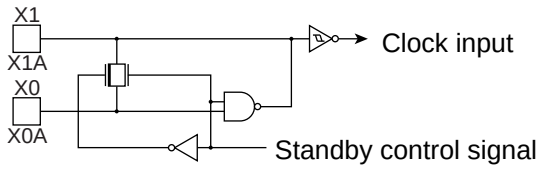
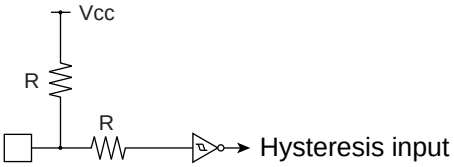
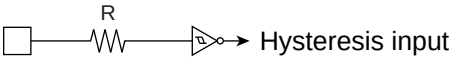
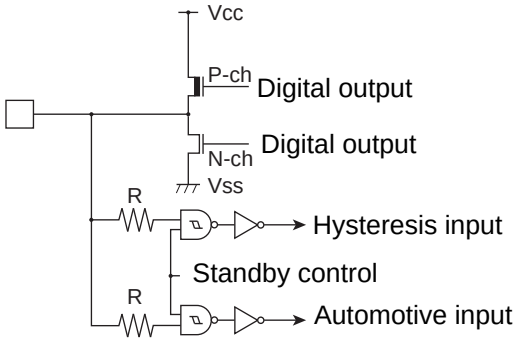
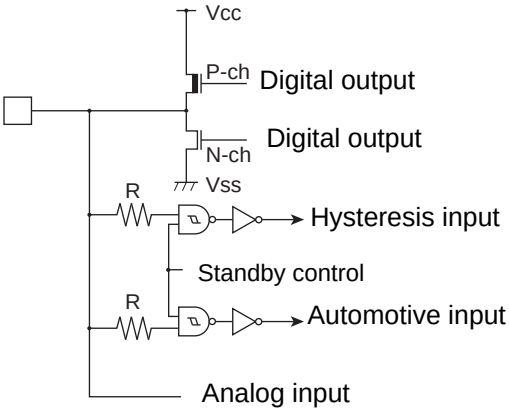
(Continued)

(Continued)

Pin No.	Pin name	Circuit type	Function
33 to 36	P14 to P17	G	General-purpose input/output ports. High-current output ports.
	PPG0 to PPG3		Functions as output pin of PPG timers 01 and 23. Valid when output setting is “enabled.”
37	P40	D	General-purpose input/output port.
	SIN1		Serial data input pin for UART1. Use the pin by setting as input port.
38	P41	D	General-purpose input/output port.
	SCK1		Serial clock input/output pin for UART1. Valid only when serial clock input/output setting on UART1 is “enabled.”
39	P42	D	General-purpose input/output port.
	SOT1		Serial data output pin for UART1. Valid only when serial data output setting on UART1 is “enabled.”
40	P43	D	General-purpose input/output port.
	TX		Transmission output pin for CAN. Valid only when output setting is “enabled.”
41	P44	D	General-purpose input/output port.
	RX		Receive input pin for CAN. Use the pin by setting as input port.
42	P30	D	General-purpose input/output port.
	SOT0		Serial data output pin for UART0. Valid only when serial data output setting on UART0 is “enabled.”
43	P31	D	General-purpose input/output port.
	SCK0		Serial clock input/output pin for UART0. Valid only when serial clock input/output setting on UART0 is “enabled.”
44	P32	H	General-purpose input/output port.
	SIN0		Serial data input/output pin for UART0. Use the pin by setting as input port.
45	P33	D	General-purpose input/output port.
46	X0A*	A	Pin for low-rate oscillation.
	P35*		General-purpose input/output port.
47	X1A*	A	Pin for low-rate oscillation.
	P36*		General-purpose input/output port.
48	AVss	—	Vss power supply input pin for A/D converter.

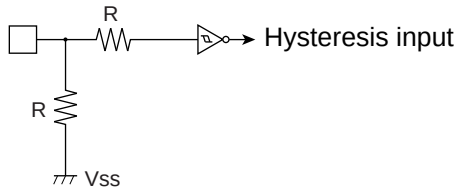
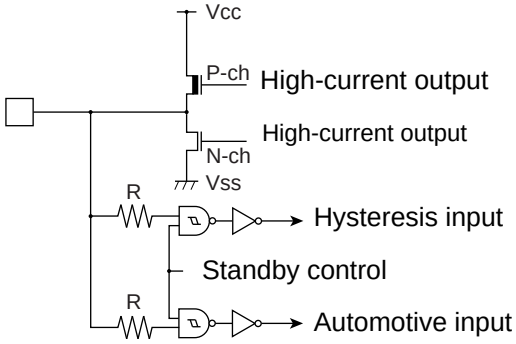
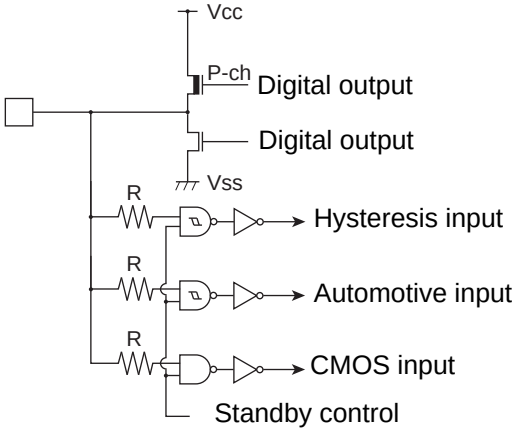
* : MB90F897/Y : X1A, X0A
MB90F897S/YS : P36, P35

■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A		• High-rate oscillation feedback resistor, approx. 1 MΩ • Low-rate oscillation feedback resistor, approx. 10 MΩ
B		• Hysteresis input with pull-up resistor. • Pull-up resistor, approx. 50 kΩ
C		Hysteresis input
D		• CMOS hysteresis input • CMOS level output • Standby control provided • Automotive input
E		• CMOS hysteresis input • CMOS level output • Shared for analog input pin • Standby control provided • Automotive input

(Continued)

(Continued)

Type	Circuit	Remarks
F		• Hysteresis input with pull-down resistor • Pull-down resistor, approx. 50 kΩ • FLASH product is not provided with pull-down resistor.
G		• CMOS hysteresis input • CMOS level output (high-current output) • Standby control provided • Automotive input
H		• CMOS hysteresis input • CMOS level output • Standby control provided • CMOS input • Automotive input

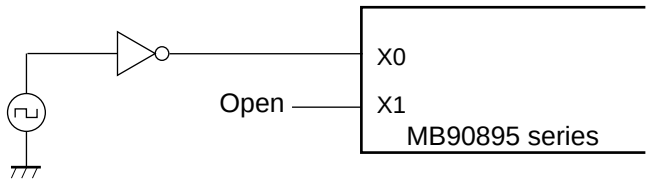
■ HANDLING DEVICES

- **Do Not Exceed Maximum Rating (preventing “latch up”)**
  - Latch-up may occur in a CMOS IC if a voltage higher than V_{CC} or less than V_{SS} is applied to an input or output pin or if a voltage exceeding the rated value is applied between V_{CC} pin and V_{SS} pins.
  - Latch-up causes drastic increase of power current, which may lead to destruction of elements by heat. Extreme caution must be taken not to exceed maximum rating.
  - When turning on and off analog power supply, take extra care not to apply an analog power voltages (AVcc and AVR) and analog input voltage that are higher than digital power voltage (Vcc).

- **Handling Unused Pins**
  - Leaving unused input pins open may cause permanent destruction by malfunction or latch-up. Apply pull-up or pull-down process to the unused pins using resistors of 2 kΩ or higher. Leave unused I/O pins open under output status, or process as input pins if they are under input status.

- **Using External Clock**
  - When using an external clock, drive only X0 pin and leave X1 pin open. An example of using an external clock is shown below.

• Using external clock



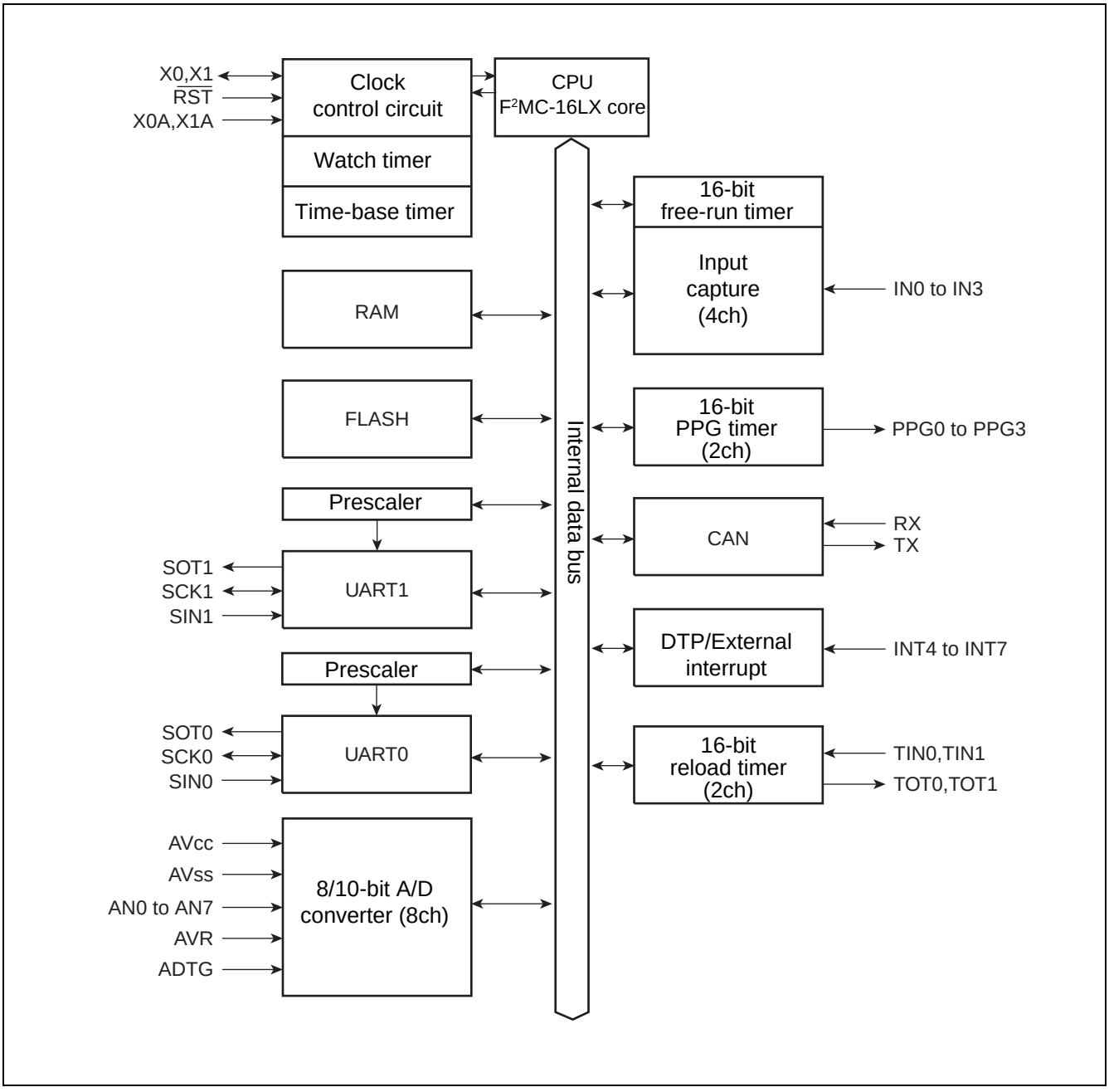
- **Notes When Using No Sub Clock on MB90F897/Y**
  - If an oscillator is not connected to X0A and X1A pins, apply pull-down resistor to the X0A pin and leave the X1A pin open.

- **About Power Supply Pins**
  - If two or more Vcc and Vss exist, the pins that should be at the same potential are connected to each other inside the device. For reducing unwanted emissions and preventing malfunction of strobe signals caused by increase of ground level, however, be sure to connect the Vcc and Vss pins to the power supply and the ground externally.
  - Pay attention to connect a power supply to Vcc and Vss pins of MB90895 series device in a lowest-possible impedance.
  - Near pins of MB90895 series device, connecting a bypass capacitor is recommended at 0.1 µF across Vcc and Vss pins.

- **Crystal Oscillator Circuit**
  - Noises around X0 and X1 pins cause malfunctions on a MB90895 series device. Design a print circuit so that X0 and X1 pins, an crystal oscillator (or a ceramic oscillator), and bypass capacitor to the ground become as close as possible to each other. Furthermore, avoid wires to X0 and X1 pins crossing each other as much as possible.
  - Print circuit designing that surrounds X0 and X1 pins with grounding wires, which ensures stable operation, is strongly recommended.

- **Caution on Operations during PLL Clock Mode**
  - If the PLL clock mode is selected, the microcontroller attempt to be working with the self-oscillating circuit even when there is no external oscillator or external clock input is stopped. Performance of this operation, however, cannot be guaranteed.
- **Sequence of Turning on Power of A/D Converter and Applying Analog Input**
  - Be sure to turn on digital power (Vcc) before applying signals to the A/D converter and applying analog input signals (AN0 to AN7 pins).
  - Be sure to turn off the power of A/D converter and analog input before turning off the digital power supply.
  - Be sure not to apply AVR exceeding AVcc when turning on and off. (No problems occur if analog and digital power is turned on and off simultaneously.)
- **Handling Pins When A/D Converter is Not Used**
  - If the A/D converter is not used, connect the pins under the following conditions: “AVcc=AVR=Vcc,” and “AVss=Vss”.
- **Note on Turning on Power**
  - For preventing malfunctions on built-in step-down circuit, maintain a minimum of 50 µs of voltage rising time (between 0.2 V and 2.7 V) when turning on the power.
- **Stabilization of supply voltage**
  - A sudden change in the supply voltage may cause the device to malfunction even within the specified V_{CC} supply voltage operating range. Therefore, the V_{CC} supply voltage should be stabilized.
    For reference, the supply voltage should be controlled so that V_{CC} ripple variations (peak-to-peak values) at commercial frequencies (50 / 60Hz) fall below 10% of the standard V_{CC} supply voltage and the coefficient of fluctuation does not exceed 0.1 V/ms at instantaneous power switching.
- **Support for +125°C / +150°C**
  - Users considering application exceeding T_A = +105°C are advised to contact their representatives beforehand for reliability limitations.

■ BLOCK DIAGRAM

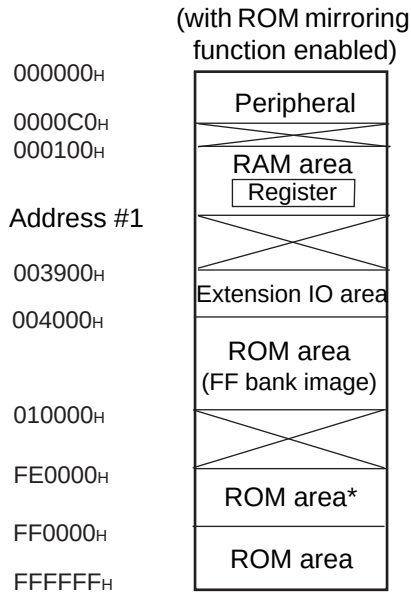


■ MEMORY MAP

1. Memory allocation of MB90895

MB90895 series model outputs 24-bit wide internal address bus and up to 24-bit of external address bus.
A maximum of 16 Mbyte memory space of external access memory is accessible.

2. Memory map



Model	Address #1
MB90V495G	001900H
MB90F897/S/Y/YS	000900H

: Internal access memory
: Access disallowed

* : On MB90F897/S/Y/YS, to read "FE0000H" to "FEFFFFH" is to read out "FF0000H" to "FFFFFFH".

Note : When internal ROM is operating, F²MC-16LX allows viewing ROM data image on FF bank at upper-level of 00 bank. This function is called "mirroring ROM," which allows effective use of C compiler small model. F²MC-16LX assigns the same low order 16-bit address to FF bank and 00 bank, which allows referencing table in ROM without specifying "far" using pointer.
For example, when accessing to "00C000H", ROM data at "FFC000H" is accessed actually. However, because ROM area of FF bank exceeds 48 Kbytes, viewing all areas is not possible on 00 bank image. Because ROM data of "FF4000H" to "FFFFFFH" is viewed on "004000H" to "00FFFFH" image, store a ROM data table in area "FF4000H" to "FFFFFFH."

■ I/O MAP

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
000000H	(Reserved area) *				
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H to 000010H	(Reserved area) *				
000011H	DDR1	Port 1 direction data register	R/W	Port 1	00000000B
000012H	DDR2	Port 2 direction data register	R/W	Port 2	00000000B
000013H	DDR3	Port 3 direction data register	R/W	Port 3	000X0000B
000014H	DDR4	Port 4 direction data register	R/W	Port 4	XXX00000B
000015H	DDR5	Port 5 direction data register	R/W	Port 5	00000000B
000016H to 00001AH	(Reserved area) *				
00001BH	ADER	Analog input permission register	R/W	8/10-bit A/D converter	11111111B
00001CH to 00001FH	(Reserved area) *				
000020H	SMR0	Serial mode register 0	R/W	UART0	00000000B
000021H	SCR0	Serial control register 0	R/W, W		00000100B
000022H	SIDR0/ SODR0	Serial input data register 0/ Serial output data register 0	R, W		XXXXXXXXB
000023H	SSR0	Serial status register 0	R, R/W		00001X00B
000024H	CDCR0	Communication prescaler control register 0	R/W		0XXX1111B
000025H	SES0	Serial edge selection register 0	R/W		XXXXXXX0B
000026H	SMR1	Serial mode register 1	R/W	UART1	00000000B
000027H	SCR1	Serial control register 1	R/W, W		00000100B
000028H	SIDR1/ SODR1	Serial input data register 1/ Serial output data register 1	R, W		XXXXXXXXB
000029H	SSR1	Serial status data register 1	R, R/W		00001000B
00002AH	(Reserved area) *				
00002BH	CDCR1	Communication prescaler control register 1	R/W	UART1	0XXX0000B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
00002C$_H$ to 00002F$_H$	(Reserved area) *				
000030$_H$	ENIR	DTP/External interrupt permission register	R/W	DTP/External interrupt	00000000$_B$
000031$_H$	EIRR	DTP/External interrupt source register	R/W		XXXXXXXX$_B$
000032$_H$	ELVR	Detection level setting register	R/W		00000000$_B$
000033$_H$			R/W		00000000$_B$
000034$_H$	ADCS	A/D control status register	R/W	8/10-bit A/D converter	00000000$_B$
000035$_H$			R/W, W		00000000$_B$
000036$_H$	ADCR	A/D data register	W, R		XXXXXXXX$_B$
000037$_H$			R		00101XXX$_B$
000038$_H$ to 00003E$_H$	(Reserved area) *				
00003F$_H$	PSCCR	PLL/Subclock control register	R/W, W	Clock	XXXX0000$_B$
000040$_H$	PPGC0	PPG0 operation mode control register	R/W, W	8/16-bit PPG timer 0/1	0X000XX1$_B$
000041$_H$	PPGC1	PPG1 operation mode control register	R/W, W		0X000001$_B$
000042$_H$	PPG01	PPG0/1 count clock selection register	R/W		000000XX$_B$
000043$_H$	(Reserved area) *				
000044$_H$	PPGC2	PPG2 operation mode control register	R/W, W	8/16-bit PPG timer 2/3	0X000XX1$_B$
000045$_H$	PPGC3	PPG3 operation mode control register	R/W, W		0X000001$_B$
000046$_H$	PPG23	PPG2/3 count clock selection register	R/W		000000XX$_B$
000047$_H$ to 00004F$_H$	(Reserved area) *				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
000050H	IPCP0	Input capture data register 0	R	16-bit input/output timer	XXXXXXXXB
000051H					XXXXXXXXB
000052H	IPCP1	Input capture data register 1	R		XXXXXXXXB
000053H					XXXXXXXXB
000054H	ICS01	Input capture control status register	R/W		00000000B
000055H	ICS23				00000000B
000056H	TCDT	Timer counter data register	R/W		00000000B
000057H					00000000B
000058H	TCCS	Timer counter control status register	R/W		00000000B
000059H	(Reserved area) *				
00005AH	IPCP2	Input capture data register 2	R	16-bit input/output timer	XXXXXXXXB
00005BH					XXXXXXXXB
00005CH	IPCP3	Input capture data register 3	R		XXXXXXXXB
00005DH					XXXXXXXXB
00005EH to 000065H	(Reserved area) *				
000066H	TMCSR0	Timer control status register	R/W	16-bit reload timer 0	00000000B
000067H			R/W		XXXX0000B
000068H	TMCSR1		R/W	16-bit reload timer 1	00000000B
000069H			R/W		XXXX0000B
00006AH to 00006EH	(Reserved area) *				
00006FH	ROMM	ROM mirroring function selection register	W	ROM mirroring function selection module	XXXXXXX1B
000070H to 00007FH	(Reserved area) *				
000080H	BVALR	Message buffer enabling register	R/W	CAN controller	00000000B
000081H	(Reserved area) *				
000082H	TREQR	Send request register	R/W	CAN controller	00000000B
000083H	(Reserved area) *				
000084H	TCANR	Send cancel register	W	CAN controller	00000000B
000085H	(Reserved area) *				
000086H	TCR	Send completion register	R/W	CAN controller	00000000B

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
000087H	(Reserved area) *				
000088H	RCR	Receive completion register	R/W	CAN controller	00000000B
000089H	(Reserved area) *				
00008AH	RRTRR	Receive RTR register	R/W	CAN controller	00000000B
00008BH	(Reserved area) *				
00008CH	ROVRR	Receive overrun register	R/W	CAN controller	00000000B
00008DH	(Reserved area) *				
00008EH	RIER	Receive completion interrupt permission register	R/W	CAN controller	00000000B
00008FH to 00009DH	(Reserved area) *				
00009EH	PACSR	Address detection control register	R/W	Address matching detection function	00000000B
00009FH	DIRR	Delay interrupt request generation/ release register	R/W	Delay interrupt generation module	XXXXXXX0B
0000A0H	LPMCR	Lower power consumption mode control register	W,R/W	Lower power consumption mode	00011000B
0000A1H	CKSCR	Clock selection register	R,R/W	Clock	11111100B
0000A2H	PILR	Port input level selection register	R/W	I/O	0000000XB
0000A3H to 0000A7H	(Reserved area) *				
0000A8H	WDTC	Watchdog timer control register	R,W	Watchdog timer	XXXXX111B
0000A9H	TBTC	Time-base timer control register	R/W,W	Time-base timer	1XX00100B
0000AAH	WTC	Watch timer control register	R,R/W	Watch timer	1X001000B
0000ABH to 0000ADH	(Reserved area) *				
0000AEH	FMCS	Flash memory control status register	R,W,R/W	512K-bit flash memory	000X0000B
0000AFH	(Reserved area) *				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
0000B0H	ICR00	Interrupt control register 00	R/W	Interrupt controller	00000111B
0000B1H	ICR01	Interrupt control register 01			00000111B
0000B2H	ICR02	Interrupt control register 02			00000111B
0000B3H	ICR03	Interrupt control register 03			00000111B
0000B4H	ICR04	Interrupt control register 04			00000111B
0000B5H	ICR05	Interrupt control register 05			00000111B
0000B6H	ICR06	Interrupt control register 06			00000111B
0000B7H	ICR07	Interrupt control register 07			00000111B
0000B8H	ICR08	Interrupt control register 08			00000111B
0000B9H	ICR09	Interrupt control register 09			00000111B
0000BAH	ICR10	Interrupt control register 10			00000111B
0000BBH	ICR11	Interrupt control register 11			00000111B
0000BCH	ICR12	Interrupt control register 12			00000111B
0000BDH	ICR13	Interrupt control register 13			00000111B
0000BEH	ICR14	Interrupt control register 14			00000111B
0000BFH	ICR15	Interrupt control register 15			00000111B
0000C0H to 0000FFH	(Reserved area) *				
001FF0H	PADR0	Detection address setting register 0 (low-order)	R/W	Address matching detection function	XXXXXXXXB
001FF1H		Detection address setting register 0 (middle-order)			XXXXXXXXB
001FF2H		Detection address setting register 0 (high-order)			XXXXXXXXB
001FF3H	PADR1	Detection address setting register 1 (low-order)	R/W		XXXXXXXXB
001FF4H		Detection address setting register 1 (middle-order)			XXXXXXXXB
001FF5H		Detection address setting register 1 (high-order)			XXXXXXXXB
003900H	TMR0/ TMRLR0	16-bit timer register 0/16-bit reload register 0	R,W	16-bit reload timer 0	XXXXXXXXB
003901H					XXXXXXXXB
003902H	TMR1/ TMRLR1	16-bit timer register 1/16-bit reload register 1	R,W	16-bit reload timer 1	XXXXXXXXB
003903H					XXXXXXXXB
003904H to 003909H	(Reserved area) *				

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
00390A$_H$	FWR0	FLASH programing control register 0	R/W	Dual operation FLASH	00000000$_B$
00390B$_H$	FWR1	FLASH programing control register 1	R/W		00000000$_B$
00390C$_H$	SSR0	Sector conversion set register	R/W		00XXXXX0$_B$
00390D$_H$ to 00390F$_H$	(Reserved area) *				
003910$_H$	PRLL0	PPG0 reload register L	R/W	8/16-bit PPG timer	XXXXXXXX$_B$
003911$_H$	PRLH0	PPG0 reload register H	R/W		XXXXXXXX$_B$
003912$_H$	PRLL1	PPG1 reload register L	R/W		XXXXXXXX$_B$
003913$_H$	PRLH1	PPG1 reload register H	R/W		XXXXXXXX$_B$
003914$_H$	PRLL2	PPG2 reload register L	R/W		XXXXXXXX$_B$
003915$_H$	PRLH2	PPG2 reload register H	R/W		XXXXXXXX$_B$
003916$_H$	PRLL3	PPG3 reload register L	R/W		XXXXXXXX$_B$
003917$_H$	PRLH3	PPG3 reload register H	R/W		XXXXXXXX$_B$
003918$_H$ to 00392F$_H$	(Reserved area) *				
003930$_H$ to 003BFF$_H$	(Reserved area) *				
003C00$_H$ to 003C0F$_H$	RAM (General-purpose RAM)				
003C10$_H$ to 003C13$_H$	IDR0	ID register 0	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003C14$_H$ to 003C17$_H$	IDR1	ID register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C18$_H$ to 003C1B$_H$	IDR2	ID register 2	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C1C$_H$ to 003C1F$_H$	IDR3	ID register 3	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C20$_H$ to 003C23$_H$	IDR4	ID register 4	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C24$_H$ to 003C27$_H$	IDR5	ID register 5	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C28$_H$ to 003C2B$_H$	IDR6	ID register 6	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
003C2C$_H$ to 003C2F$_H$	IDR7	ID register 7	R/W	CAN controller	XXXXXXXX$_B$ to XXXXXXXX$_B$
003C30$_H$ 003C31$_H$	DLCR0	DLC register 0	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C32$_H$ 003C33$_H$	DLCR1	DLC register 1	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C34$_H$ 003C35$_H$	DLCR2	DLC register 2	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C36$_H$ 003C37$_H$	DLCR3	DLC register 3	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C38$_H$ 003C39$_H$	DLCR4	DLC register 4	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C3A$_H$ 003C3B$_H$	DLCR5	DLC register 5	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C3C$_H$ 003C3D$_H$	DLCR6	DLC register 6	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C3E$_H$ 003C3F$_H$	DLCR7	DLC register 7	R/W		XXXXXXXX$_B$ XXXXXXXX$_B$
003C40$_H$ to 003C47$_H$	DTR0	Data register 0	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C48$_H$ to 003C4F$_H$	DTR1	Data register 1	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C50$_H$ to 003C57$_H$	DTR2	Data register 2	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C58$_H$ to 003C5F$_H$	DTR3	Data register 3	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C60$_H$ to 003C67$_H$	DTR4	Data register 4	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C68$_H$ to 003C6F$_H$	DTR5	Data register 5	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C70$_H$ to 003C77$_H$	DTR6	Data register 6	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$
003C78$_H$ to 003C7F$_H$	DTR7	Data register 7	R/W		XXXXXXXX$_B$ to XXXXXXXX$_B$

(Continued)

(Continued)

Address	Register abbreviation	Register	Read/ Write	Resource	Initial value
003C80H to 003CFFH	(Reserved area) *				
003D00H 003D01H	CSR	Control status register	R/W, R	CAN controller	0XXXX001B 00XXX000B
003D02H	LEIR	Last event display register	R/W		000XX000B
003D03H	(Reserved area) *				
003D04H 003D05H	RTEC	Send/receive error counter	R	CAN controller	00000000B 00000000B
003D06H 003D07H	BTR	Bit timing register	R/W		11111111B X1111111B
003D08H	IDER	IDE register	R/W		XXXXXXXXB
003D09H	(Reserved area) *				
003D0AH	TRTRR	Send RTR register	R/W		00000000B
003D0BH	(Reserved area) *				
003D0CH	RFWTR	Remote frame receive wait register	R/W	CAN controller	XXXXXXXXB
003D0DH	(Reserved area) *				
003D0EH	TIER	Send completion interrupt permission register	R/W	CAN controller	00000000B
003D0FH	(Reserved area) *				
003D10H 003D11H	AMSR	Acceptance mask selection register	R/W	CAN controller	XXXXXXXXB XXXXXXXXB
003D12H 003D13H	(Reserved area) *				
003D14H to 003D17H	AMR0	Acceptance mask register 0	R/W	CAN controller	XXXXXXXXB to XXXXXXXXB
003D18H to 003D1BH	AMR1	Acceptance mask register 1	R/W		XXXXXXXXB to XXXXXXXXB
003D1CH to 003DFFH	(Reserved area) *				
003E00H to 003EFFH	(Reserved area) *				
003FF0H to 003FFFH	(Reserved area) *				

Initial values :

0 : Initial value of this bit is “0.”

1 : Initial value of this bit is “1.”

X : Initial value of this bit is undefined.

* : “Reserved area” should not be written anything. Result of reading from “Reserved area” is undefined.

■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS

Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority*3
		Number		Address	ICR	Address	
Reset	×	#08	08H	FFFFDCH	—	—	High
INT 9 instruction	×	#09	09H	FFFFD8H	—	—	↑
Exceptional treatment	×	#10	0AH	FFFFD4H	—	—	
CAN controller reception completed (RX)	×	#11	0BH	FFFFD0H	ICR00	0000B0H*1	
CAN controller transmission completed (TX) / Node status transition (NS)	×	#12	0CH	FFFFCCH			
Reserved	×	#13	0DH	FFFFC8H	ICR01	0000B1H	
Reserved	×	#14	0EH	FFFFC4H			
CAN wakeup	Δ	#15	0FH	FFFFC0H	ICR02	0000B2H*1	
Time-base timer	×	#16	10H	FFFFBCH			
16-bit reload timer 0	Δ	#17	11H	FFFFB8H	ICR03	0000B3H*1	
8/10-bit A/D converter	Δ	#18	12H	FFFFB4H			
16-bit free-run timer overflow	Δ	#19	13H	FFFFB0H	ICR04	0000B4H*1	
Reserved	×	#20	14H	FFFFACH			
Reserved	×	#21	15H	FFFFA8H	ICR05	0000B5H*1	
PPG timer ch.0, ch.1 underflow	×	#22	16H	FFFFA4H			
Input capture 0-input	Δ	#23	17H	FFFFA0H	ICR06	0000B6H*1	
External interrupt (INT4/INT5)	Δ	#24	18H	FFFF9CH			
Input capture 1-input	Δ	#25	19H	FFFF98H	ICR07	0000B7H*2	
PPG timer ch.2, ch.3 underflow	×	#26	1AH	FFFF94H			
External interrupt (INT6/INT7)	Δ	#27	1BH	FFFF90H	ICR08	0000B8H*1	
Watch timer	Δ	#28	1CH	FFFF8CH			
Reserved	×	#29	1DH	FFFF88H	ICR09	0000B9H*1	
Input capture 2-input Input capture 3-input	×	#30	1EH	FFFF84H			
Reserved	×	#31	1FH	FFFF80H	ICR10	0000BAH*1	
Reserved	×	#32	20H	FFFF7CH			
Reserved	×	#33	21H	FFFF78H	ICR11	0000BBH*1	
Reserved	×	#34	22H	FFFF74H			
Reserved	×	#35	23H	FFFF70H	ICR12	0000BCH*1	↓
16-bit reload timer 1	○	#36	24H	FFFF6CH			Low

(Continued)

(Continued)

Interrupt source	EI²OS readiness	Interrupt vector			Interrupt control register		Priority*3
		Number		Address	ICR	Address	
UART1 reception completed	◎	#37	25H	FFFF68H	ICR13	0000BDH*1	High ↑
UART1 transmission completed	Δ	#38	26H	FFFF64H			
UART0 reception completed	◎	#39	27H	FFFF60H	ICR14	0000BEH*1	
UART0 transmission completed	Δ	#40	28H	FFFF5CH			
Flash memory	×	#41	29H	FFFF58H	ICR15	0000BFH*1	
Delay interrupt generation module	×	#42	2AH	FFFF54H			↓ Low

○ : Available

× : Unavailable

◎ : Available, EI²OS stop function is provided.

Δ : Available when a cause of interrupt sharing a same ICR is not used.

*1 :
- Peripheral functions sharing an ICR register have the same interrupt level.
- If peripheral functions share an ICR register, only one function is available when using extended intelligent I/O service.
- If peripheral functions share an ICR register, a function using extended intelligent I/O service does not allow interrupt by another function.

*2 : Only input capture 1 is ready for EI²OS. Because PPG is not ready for EI²OS, disable PPG interrupt when using EI²OS with Input capture 1.

*3 : Priority when two or more interrupts of a same level occur simultaneously.

■ FLASH MEMORY CONFIGURATION

• Sector configuration of 512 Kbit flash memory

Flash memory	CPU address	Writer address*	
SA0 (4 Kbytes)	FF0000H FF0FFFH	70000H 70FFFH	Lower Bank
SA1 (4 Kbytes)	FF1000H FF1FFFH	71000H 71FFFH	
SA2 (4 Kbytes)	FF2000H FF2FFFH	72000H 72FFFH	
SA3 (4 Kbytes)	FF3000H FF3FFFH	73000H 73FFFH	
SA4 (16 Kbytes)	FF4000H FF7FFFH	74000H 77FFFH	Upper Bank
SA5 (16 Kbytes)	FF8000H FFBFFFH	78000H 7BFFFH	
SA6 (4 Kbytes)	FFC000H FFCFFFH	7C000H 7CFFFH	
SA7 (4 Kbytes)	FFD000H FFDFFFH	7D000H 7DFFFH	
SA8 (4 Kbytes)	FFE000H FFEFFFH	7E000H 7EFFFH	
SA9 (4 Kbytes)	FFF000H FFFFFFH	7F000H 7FFFFH	

* : “Writer address” is an address equivalent to CPU address, which is used when data is written on flash memory, using parallel writer. When writing/deleting data with general-purpose writer, the writer address is used for writing and deleting.

■ ELECTRIC CHARACTERISTICS

1. Absolute Maximum Rating

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR$*2
Input voltage*1	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Output voltage*1	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*3
Maximum clamp current	I_{CLAMP}	– 2.0	+ 2.0	mA	*7
Total maximum clamp current	$\Sigma\lvert I_{CLAMP} \rvert$	—	20	mA	*7
“L” level maximum output current	I_{OL1}	—	15	mA	Normal output*4
	I_{OL2}	—	40	mA	High-current output*4
“L” level average output current	I_{OLAV1}	—	4	mA	Normal output*5
	I_{OLAV2}	—	30	mA	High-current output*5
“L” level maximum total output current	ΣI_{OL1}	—	125	mA	Normal output
	ΣI_{OL2}	—	160	mA	High-current output
“L” level average total output current	ΣI_{OLAV1}	—	40	mA	Normal output*6
	ΣI_{OLAV2}	—	40	mA	High-current output*6
“H” level maximum output current	I_{OH1}	—	–15	mA	Normal output*4
	I_{OH2}	—	–40	mA	High-current output*4
“H” level average output current	I_{OHAV1}	—	–4	mA	Normal output*5
	I_{OHAV2}	—	–30	mA	High-current output*5
“H” level maximum total output current	ΣI_{OH1}	—	–125	mA	Normal output
	ΣI_{OH2}	—	–160	mA	High-current output
“H” level average total output current	ΣI_{OHAV1}	—	–40	mA	Normal output*6
	ΣI_{OHAV2}	—	–40	mA	High-current output*6
Power consumption	P_D	—	297	mW	
Operating temperature	T_A	–40	+105	°C	Other than MB90F897Y/YS
		–40	+125	°C	*8 Other than MB90F897Y/YS
		–40	+150	°C	*8, *9 MB90F897Y/YS
Storage temperature	Tstg	–55	+150	°C	

*1: The parameter is based on $V_{SS} = AV_{SS} =$ 0.0 V.

*2 : AVcc and AVR should not exceed Vcc.

(Continued)

(Continued)

*3 : V_I and V_O should not exceed Vcc + 0.3 V. However, if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating.

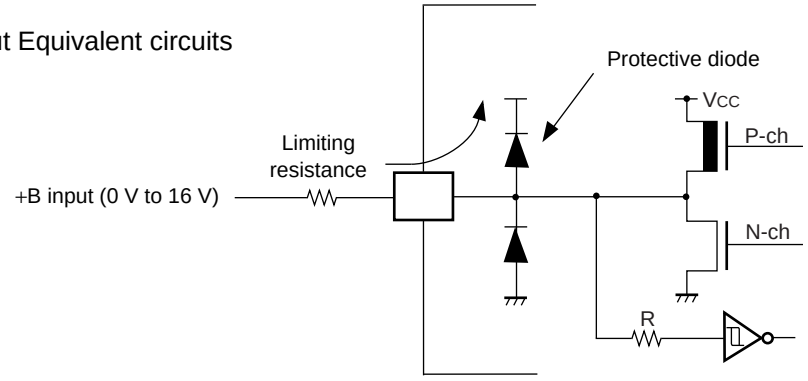
*4 : A peak value of an applicable one pin is specified as a maximum output current.

*5 : An average current value of an applicable one pin within 100 ms is specified as an average output current. (Average value is found by multiplying operating current by operating rate.)

*6 : An average current value of all pins within 100 ms is specified as an average total output current. (Average value is found by multiplying operating current by operating rate.)

*7 :
- Applicable to pins: P10 to P17, P20 to P27, P30 to P33, P35, P36, P37, P40 to P44, P50 to P57
  Note: P35 and P36 are MB90F897S/YS only.
- Use within recommended operating conditions.
- Use at DC voltage (current) .
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the V_{CC} pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0 V) , the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the power-on reset.
- Care must be taken not to leave the +B input pin open.
- Note that analog system input/output pins other than the A/D input pins (LCD drive pins, comparator input pins, etc.) cannot accept +B signal input.
- Sample recommended circuits:

• Input/Output Equivalent circuits



*8 : Users considering application exceeding T_A = +105°C are advised to contact their FUJITSU MICROELECTRONICS representatives beforehand for reliability limitations.

*9 : Use the PB circuit board which has 4 or more layers.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

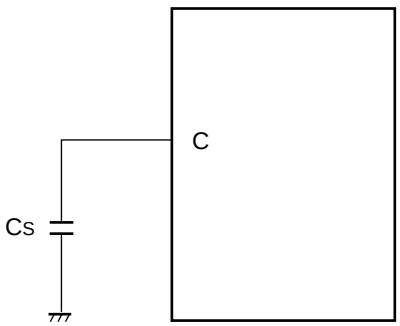
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}	3.5	5.0	5.5	V	Under normal operation
		3.0	—	5.5	V	Retain status of stop operation
		4.0	—	5.5	V	Accuracy guarantee voltage of A/D converter
Smoothing capacitor	C_S	0.1	—	1.0	µF	*1
Operating temperature	T_A	–40	—	+105	°C	Other than MB90F897Y/YS
		–40	—	+125	°C	*2 Other than MB90F897Y/YS
		–40	—	+150	°C	*2, *3 MB90F897Y/YS

*1 : Use a ceramic capacitor, or a capacitor of similar frequency characteristics. On the Vcc pin, use a bypass capacitor that has a larger capacity than that of Cs.
Refer to the following figure for connection of smoothing capacitor Cs.

*2: Users considering application exceeding T_A = +105°C are advised to contact their FUJITSU MICROELECTRONICS representatives beforehand for reliability limitations.

*3 : Use the PB circuit board which has 4 or more layers.

• C pin connection diagram



WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

• **MB90F897/S (Models that support + 125 °C)**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	When selected CMOS hysteresis
	V_{IHA}	Automotive input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	When selected Automotive
	V_{IHC}	CMOS input pin (P32, P40)	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	When selected CMOS
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	When selected CMOS hysteresis
	V_{ILA}	Automotive input pin	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	When selected Automotive
	V_{ILC}	CMOS input pin (P32, P40)	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	When selected CMOS
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OH} = –4.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P14 to P17	V_{CC} = 4.5 V, I_{OH} = –14.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OL} = 4.0 mA	—	—	0.4	V	
	V_{OL2}	P14 to P17	V_{CC} = 4.5 V, I_{OL} = 20.0 mA	—	—	0.4	V	
Input leak current	I_{IL}	All input pins	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, normal operation.	—	25	30	mA	
			V_{CC} = 5.0 V, Internally operating at 16 MHz, writing on flash memory.	—	45	50	mA	MB90F897/S
			V_{CC} = 5.0 V, Internally operating at 16 MHz, deleting on flash memory.	—	45	50	mA	MB90F897/S

* : Test conditions of power supply current are based on a device using external clock.

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCS}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, sleeping.	—	8	12	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode.	—	0.2	0.35	mA	
	I_{CTSPII}		V_{CC} = 5.0 V, Internally operating at 16 MHz, transition from PLL clock mode, in time-base timer mode.	—	3	5	mA	
	I_{CCL}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T_A = +25°C	—	40	100	µA	
	I_{CCLS}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T_A = +25°C	—	10	50	µA	
	I_{CCT}		V_{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T_A = +25°C	—	8	30	µA	
	I_{CCH}		Stopping, T_A = +25°C	—	5	25	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	—	—	5	15	pF	
Pull-up resistor	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	—	25	50	100	kΩ	FLASH product is not provided with pull-down resistor.

* : Test conditions of power supply current are based on a device using external clock.

• **MB90F897Y/YS (Models that support + 150 °C) (Under development)**

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +150 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IHS}	CMOS hysteresis input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	When selected CMOS hysteresis
	V_{IHA}	Automotive input pin	—	0.8 V_{CC}	—	V_{CC} + 0.3	V	When selected Automotive
	V_{IHC}	CMOS input pin (P32, P40)	—	0.7 V_{CC}	—	V_{CC} + 0.3	V	When selected CMOS
	V_{IHM}	MD input pin	—	V_{CC} – 0.3	—	V_{CC} + 0.3	V	
"L" level input voltage	V_{ILS}	CMOS hysteresis input pin	—	V_{SS} – 0.3	—	0.2 V_{CC}	V	When selected CMOS hysteresis
	V_{ILA}	Automotive input pin	—	V_{SS} – 0.3	—	0.5 V_{CC}	V	When selected Automotive
	V_{ILC}	CMOS input pin (P32, P40)	—	V_{SS} – 0.3	—	0.3 V_{CC}	V	When selected CMOS
	V_{ILM}	MD input pin	—	V_{SS} – 0.3	—	V_{SS} + 0.3	V	
"H" level output voltage	V_{OH1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OH} = –3.0 mA	V_{CC} – 0.5	—	—	V	
	V_{OH2}	P14 to P17	V_{CC} = 4.5 V, I_{OH} = –12.0 mA	V_{CC} – 0.5	—	—	V	
"L" level output voltage	V_{OL1}	Pins other than P14 to P17	V_{CC} = 4.5 V, I_{OL} = 3.0 mA	—	—	0.4	V	
	V_{OL2}	P14 to P17	V_{CC} = 4.5 V, I_{OL} = 16 mA	—	—	0.4	V	
Input leak current	I_{IL}	All input pins	V_{CC} = 5.5 V, V_{SS} < V_I < V_{CC}	–5	—	+5	µA	
Power supply current*	I_{CC}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, normal operation.	—	25	32	mA	
			V_{CC} = 5.0 V, Internally operating at 16 MHz, writing on flash memory. T_A = –40 °C to +125 °C	—	45	50	mA	Up to + 125 °C
			V_{CC} = 5.0 V, Internally operating at 16 MHz, deleting on flash memory. T_A = –40 °C to +125 °C	—	45	50	mA	Up to + 125 °C

* : Test conditions of power supply current are based on a device using external clock.

(Continued)

(Continued)

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +150 °C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*	I_{CCS}	V_{CC}	V_{CC} = 5.0 V, Internally operating at 16 MHz, sleeping.	—	8	14	mA	
	I_{CTS}		V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode. T_A = –40 °C to +125 °C	—	0.2	0.35	mA	Up to + 125 °C
			V_{CC} = 5.0 V, Internally operating at 2 MHz, transition from main clock mode, in time-base timer mode. T_A = +125 °C to +150 °C	—	0.2	T.B.D	mA	
	I_{CTSPII}		V_{CC} = 5.0 V, Internally operating at 16 MHz, transition from PLL clock mode, in time-base timer mode.	—	3	7	mA	
	I_{CCL}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock operation, T_A = + 25°C	—	40	100	µA	
	I_{CCLS}		V_{CC} = 5.0 V, Internally operating at 8 kHz, subclock, sleep mode, T_A = + 25°C	—	10	50	µA	
	I_{CCT}		V_{CC} = 5.0 V, Internally operating at 8 kHz, watch mode, T_A = + 25°C	—	8	30	µA	
	I_{CCH}		Stopping, T_A = + 25°C	—	5	25	µA	
Input capacity	C_{IN}	Other than AV_{CC}, AV_{SS}, AVR, C, V_{CC}, V_{SS}	—	—	5	15	pF	
Pull-up resistor	R_{UP}	$\overline{RST}$	—	25	50	100	kΩ	
Pull-down resistor	R_{DOWN}	MD2	—	25	50	100	kΩ	FLASH product is not provided with pull-down resistor.

* : Test conditions of power supply current are based on a device using external clock.

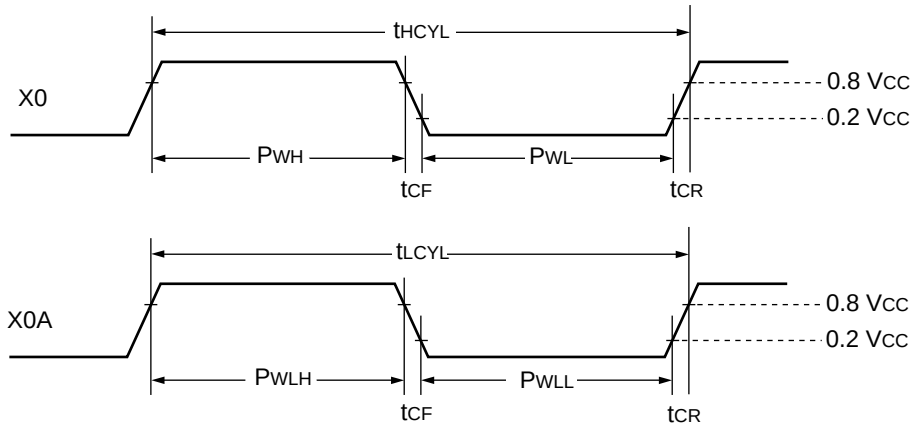
4. AC Characteristics

(1) Clock timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

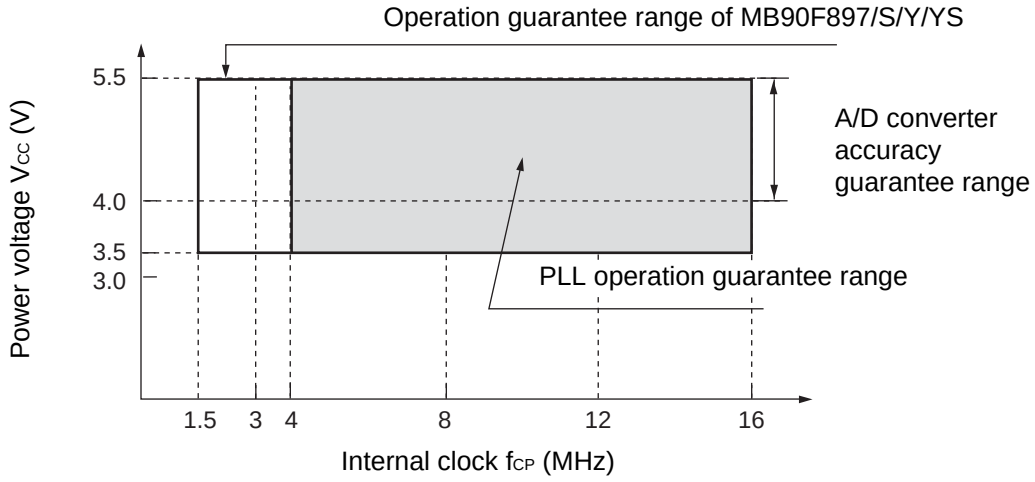
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Clock frequency	f_C	X0, X1	3	—	8	MHz	When crystal or ceramic resonator is used
			3	—	16	MHz	External clock
			4	—	16	MHz	PLL multiplied by 1
			4	—	8	MHz	PLL multiplied by 2
			4	—	5.33	MHz	PLL multiplied by 3
			4	—	4	MHz	PLL multiplied by 4
	f_{CL}	X0A, X1A	—	32.768	—	kHz	MB90F897/Y only
Clock cycle time	t_{HCYL}	X0, X1	125	—	333	ns	
	t_{LCYL}	X0A, X1A	—	30.5	—	µs	MB90F897/Y only
Input clock pulse width	P_{WH}, P_{WL}	X0	10	—	—	ns	Set duty factor at 30% to 70% as a guideline.
	P_{WLH},P_{WLL}	X0A	—	15.2	—	µs	MB90F897/Y only
Input clock rise time and fall time	t_{CR}, t_{CF}	X0	—	—	5	ns	When external clock is used
Internal operation clock frequency	f_{CP}	—	1.5	—	16	MHz	When main clock is used
	f_{LCP}	—	—	8.192	—	kHz	When sub clock is used, MB90F897/Y only
Internal operation clock cycle time	t_{CP}	—	62.5	—	666	ns	When main clock is used
	t_{LCP}	—	—	122.1	—	µs	When sub clock is used, MB90F897/Y only

• Clock timing

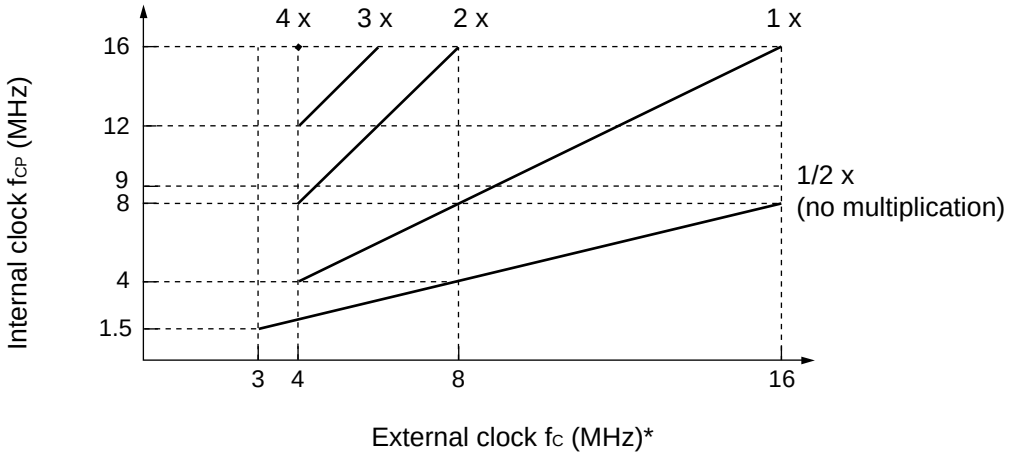


• PLL operation guarantee range

Relation between internal operation clock frequency and power supply voltage



Relation among external clock frequency and internal clock frequency

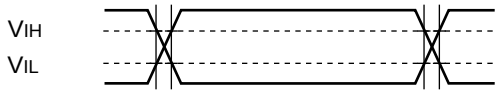


* : fc is 8 MHz at maximum when crystal or ceramic resonator circuit is used.

Rating values of alternating current is defined by the measurement reference voltage values shown below:

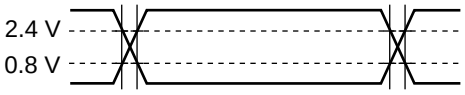
- Input signal waveform

Hysteresis input pin



- Output signal waveform

Output pin



(2) Reset input timing

(V_{CC} = 5.0 V±10%, V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

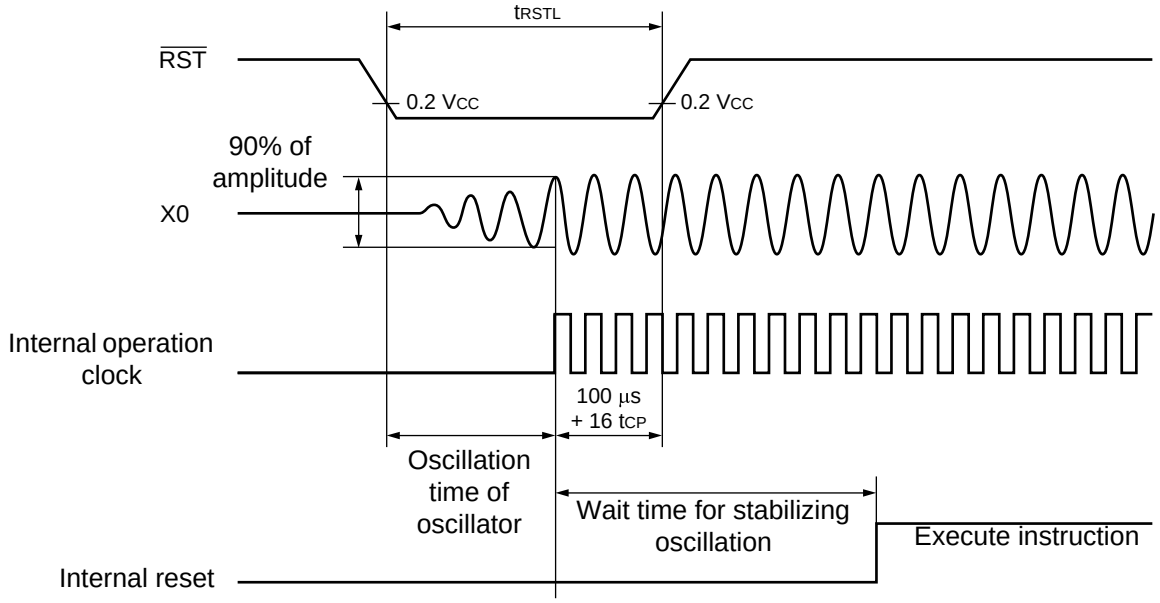
Parameter	Symbol	Pin name	Condi-tions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}*3	—	ns	Normal operation
				Oscillation time of oscillator*1 + 100 µs + 16 t_{CP}*3	—	—	In sub clock*2, sub sleep*2, watch*2 and stop mode
				100	—	µs	In timebase timer

*1 : Oscillation time of oscillator is time that the amplitude reached the 90%. In the crystal oscillator, the oscillation time is between several ms to tens of ms. In ceramic oscillator, the oscillation time is between hundreds of µs to several ms. In the external clock, the oscillation time is 0 ms.

*2 : Except for MB90F897S/YS.

*3 : Refer to “(1) Clock timing” ratings for t_{CP} (internal operation clock cycle time).

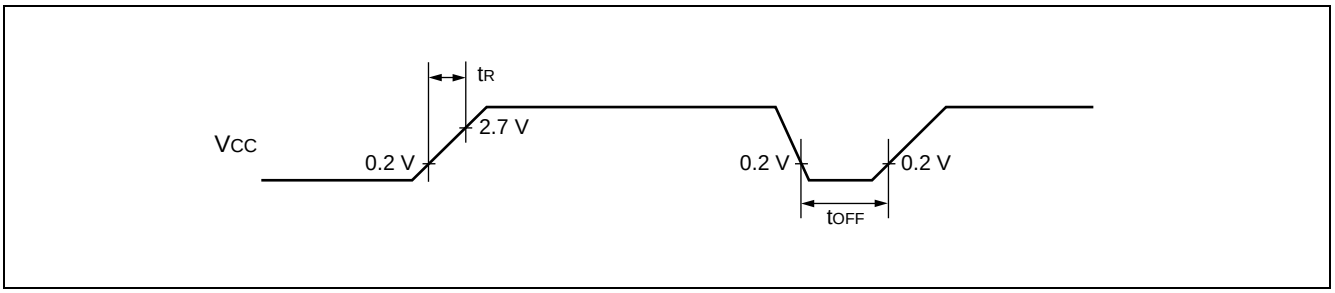
- In sub clock, sub sleep, watch and stop mode



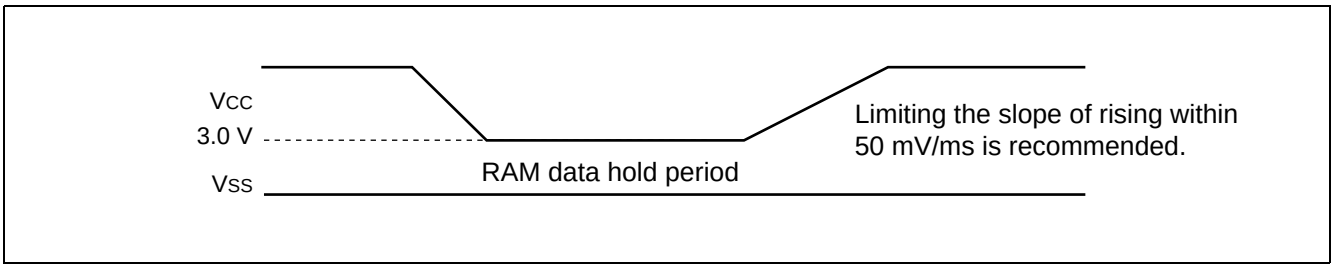
(3) Power-on reset

(V_{SS} = AV_{SS} = 0.0 V, T_A = –40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply rise time	t_R	V_{CC}	—	0.05	30	ms	
Power supply shutdown time	t_{OFF}	V_{CC}		1	—	ms	Repeated operation



Note : Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, raise the power smoothly by suppressing variation of voltages as shown below. When raising the power, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.



(4) UART0/UART1 timing

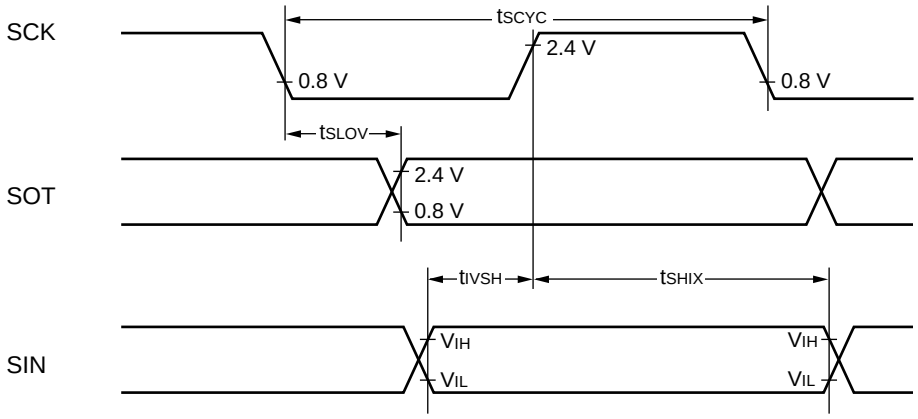
(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK0/SCK1	Internal shift clock mode output pin is : C_L = 80 pF+1TTL	8 t_{CP} *	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0/SCK1, SOT0/SOT1		–80	+80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0/SCK1, SIN0/SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0/SCK1, SIN0/SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0/SCK1	External shift clock mode output pin is : C_L = 80 pF+1TTL	4 t_{CP} *	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0/SCK1		4 t_{CP} *	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0/SCK1, SOT0/SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0/SCK1, SIN0/SIN1		60	—	ns	
SCK ↑ →valid SIN hold time	t_{SHIX}	SCK0/SCK1, SIN0/SIN1		60	—	ns	

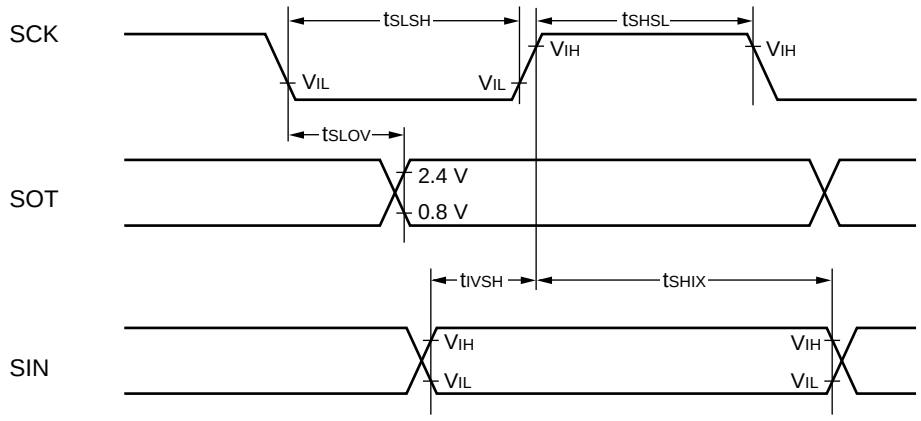
* : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

Notes: • AC rating in CLK synchronous mode.
• C_L is a load capacitance value on pins for testing.

• Internal shift clock mode



• External shift clock mode



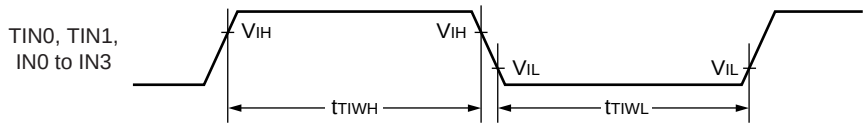
(5) Timer input timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}	TIN0, TIN1	—	4 t_{CP} *	—	ns	
	t_{TIWL}	IN0 to IN3					

* : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

• Timer input timing



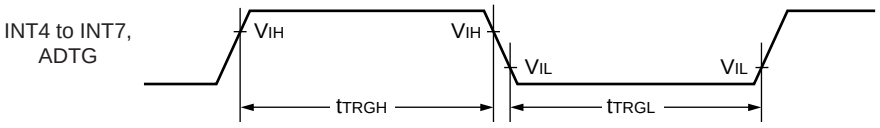
(6) Trigger input timing

(V_{CC} = 4.5 V to 5.5 V, V_{SS} = 0.0 V, T_A = –40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH} t_{TRGL}	INT4 to INT7, ADTG	—	3 t_{CP} *	—	ns	

* : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

• Trigger input timing



5. A/D converter

(V_{CC} = AV_{CC} = 5.0 V ± 10 %, 3.0 V ≤ AVR − AV_{SS}, V_{SS} = AV_{SS} = 0.0 V,
T_A = −40 °C to +125 °C/+150 °C (only MB90F897Y/YS))

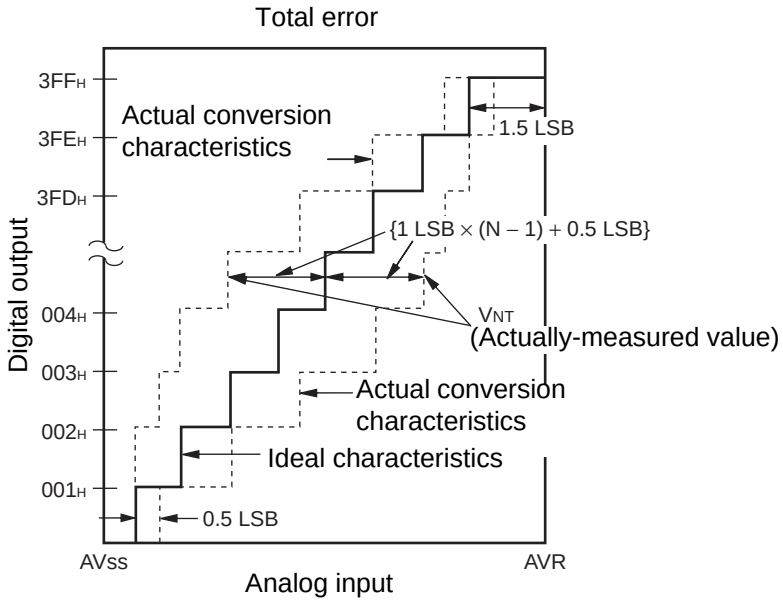
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	± 3.0	LSB	
Nonlinear error	—	—	—	—	± 2.5	LSB	
Differential linear error	—	—	—	—	± 1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} − 1.5 LSB	AV_{SS} + 0.5 LSB	AV_{SS} + 2.5 LSB	V	1 LSB = (AVR − AV_{SS}) /1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR − 3.5 LSB	AVR − 1.5 LSB	AVR + 0.5 LSB	V	
Compare time	—	—	66 t_{CP} *1	—	—	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			88 t_{CP} *1	—	—	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Sampling time	—	—	32 t_{CP} *1	—	—	ns	With 16 MHz machine clock 5.5 V ≥ AV_{CC} ≥ 4.5 V
			128 t_{CP} *1	—	—	ns	With 16 MHz machine clock 4.5 V > AV_{CC} ≥ 4.0 V
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	AV_{SS}	—	AVR	V	
Reference voltage	—	AVR	AV_{SS} + 2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	3.5	7.5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*2
Reference voltage supplying current	I_R	AVR	—	165	250	µA	
	I_{RH}	AVR	—	—	5	µA	*2
Variation among channels	—	AN0 to AN7	—	—	4	LSB	

*1 : Refer to "(1) Clock timing" ratings for t_{CP} (internal operation clock cycle time).

*2 : If A/D converter is not operating, a current when CPU is stopped is applicable (Vcc=AVcc=AVR=5.0 V).

6. Definition of A/D Converter Terms

Resolution	: Analog variation that is recognized by an A/D converter.
Linear error	: Deviation between a line across zero-transition line (“00 0000 0000” ←→“00 0000 0001”) and full-scale transition line (“11 1111 1110” ←→ “11 1111 1111”) and actual conversion characteristics.
Differential linear error	: Deviation of input voltage, which is required for changing output code by 1 LSB, from an ideal value.
Total error	: Difference between an actual value and an ideal value. A total error includes zero transition error, full-scale transition error, and linear error.



$$\text{Total error of digital output “N”} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + 0.5\ \text{LSB}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$1\ \text{LSB} = (\text{Ideal value})\ \frac{AVR - AV_{SS}}{1024}\ [\text{V}]$$

V_{OT} (Ideal value) $= AV_{SS} + 0.5$ LSB [V]

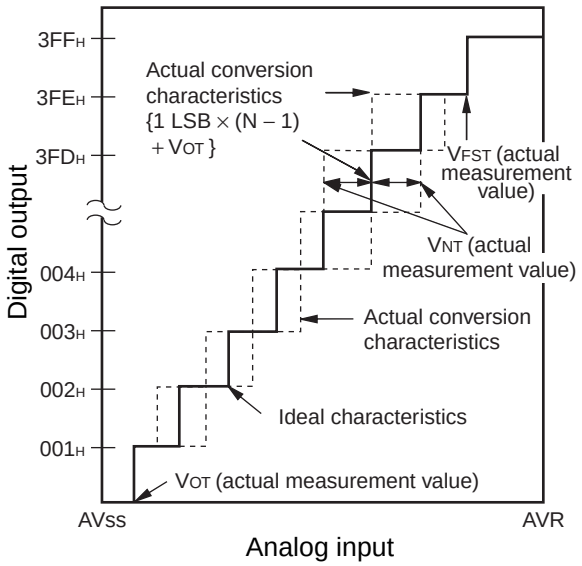
V_{FST} (Ideal value) $= AVR - 1.5$ LSB [V]

V_{NT} : A voltage at which digital output transits from (N-1) to N.

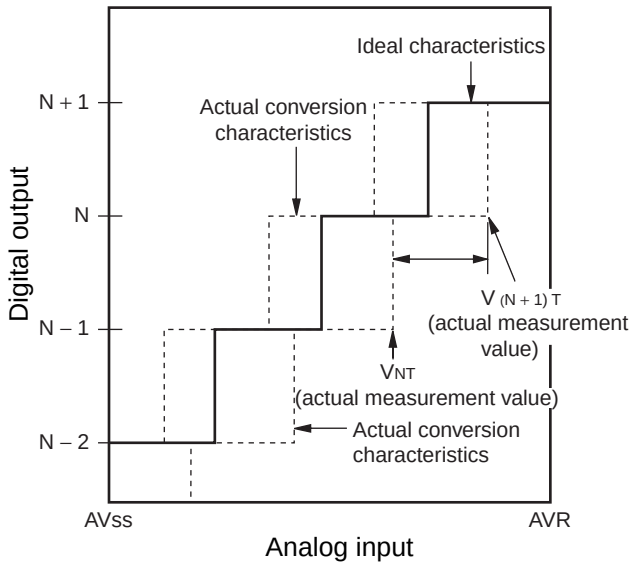
(Continued)

(Continued)

Linear error



Differential linear error



$$\text{Linear error of digital output N} = \frac{V_{NT} - \{1\ \text{LSB} \times (N - 1) + V_{OT}\}}{1\ \text{LSB}}\ [\text{LSB}]$$

$$\text{Differential linear error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1\ \text{LSB}} - 1\text{LSB}\ [\text{LSB}]$$

$$1\ \text{LSB} = \frac{V_{FST} - V_{OT}}{1022}\ [\text{V}]$$

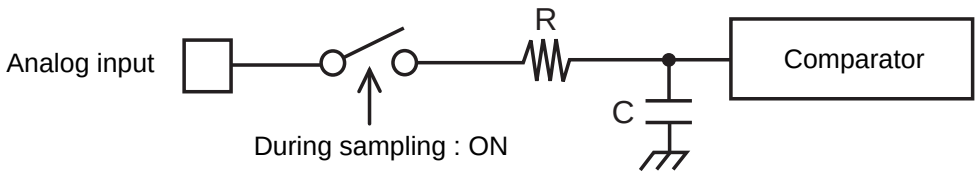
V_{OT} : Voltage at which digital output transits from “000_H” to “001_H.”
V_{FST} : Voltage at which digital output transits from “$3FE_H$” to “$3FF_H$.”

7. Notes on A/D Converter Section

<About the external impedance of the analog input and its sampling time>

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

Analog input circuit model



	R	C
MB90F897/S MB90F897Y/YS		
4.5 V ≤ AV_{CC} ≤ 5.5 V	2.4 kΩ (Max)	36.4 pF (Max)
4.0 V ≤ AV_{CC} < 4.5 V	16.4 kΩ (Max)	36.4 pF (Max)

Note : The values are reference values.

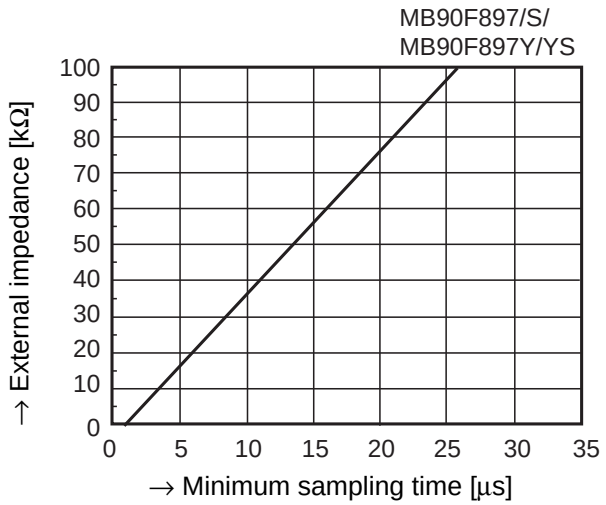
(Continued)

(Continued)

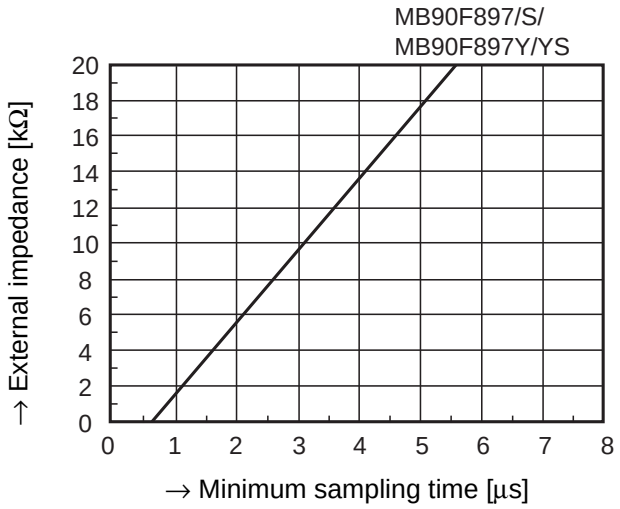
- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

(At 4.5 V ≤ AVcc ≤ 5.5 V)

[External impedance = 0 kΩ to 100 kΩ]

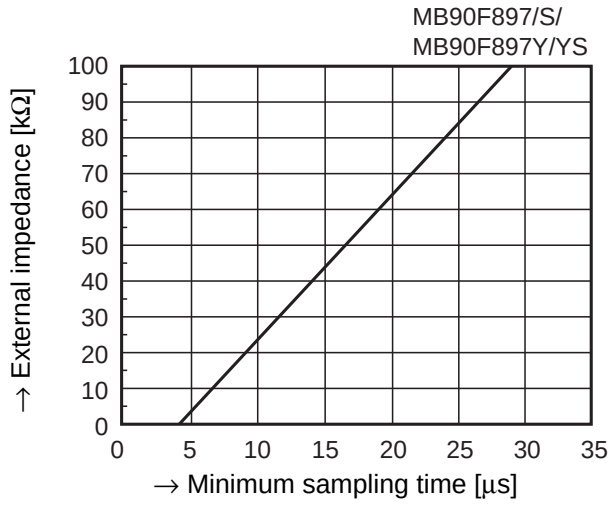


[External impedance = 0 kΩ to 20 kΩ]

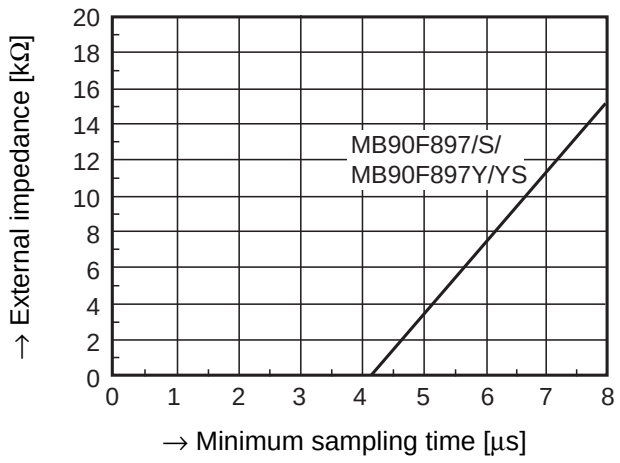


(At 4.0 V ≤ AVcc < 4.5 V)

[External impedance = 0 kΩ to 100 kΩ]



[External impedance = 0 kΩ to 20 kΩ]



The relationship between the external impedance and minimum sampling time

- If the sampling time cannot be sufficient, connect a capacitor of about 0.1 µF to the analog input pin.

<About errors>

- As |AVR – AVss| become smaller, values of relative errors grow larger.

8. Flash Memory Program/Erase Characteristics*1

Parameter	Conditions	Value			Unit	Remarks
		Min	Typ	Max		
Sector erase time (4 KB sector)	T_A = + 25 °C, V_{CC} = 5.0 V	—	0.2	0.5	s	Excludes 00_H programming prior to erasure
Sector erase time (16 KB sector)		—	0.5	7.5	s	Excludes 00_H programming prior to erasure
Chip erase time		—	2.6	—	s	Excludes 00_H programming prior to erasure
Word (16 bit width) programming time		—	16	3,600	µs	Except for the over head time of the system
Program/Erase cycle	—	10,000	—	—	cycle	
Flash Data Retention Time	Average T_A = + 85 °C	20	—	—	Years	*2

*1 : For MB90F897Y/YS, it is prohibited to write or erase data in the range of T_A = + 125 °C to + 150 °C.

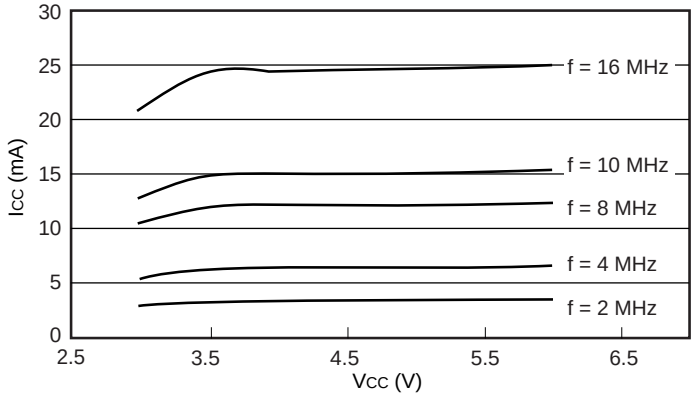
*2 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85 °C) .

■ EXAMPLE CHARACTERISTICS

• **MB90F897**

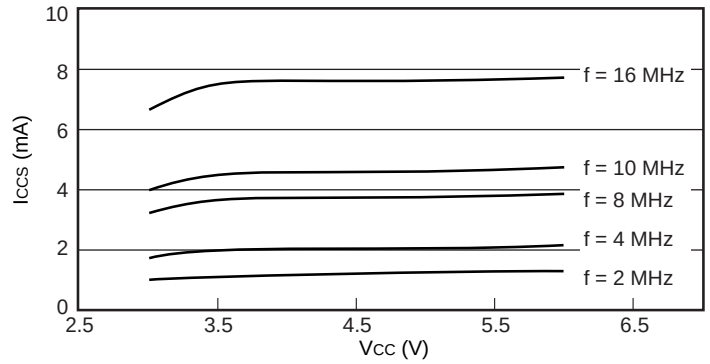
$I_{CC} - V_{CC}$

T_A = +25 °C, In external clock operation
f = Internal operating frequency



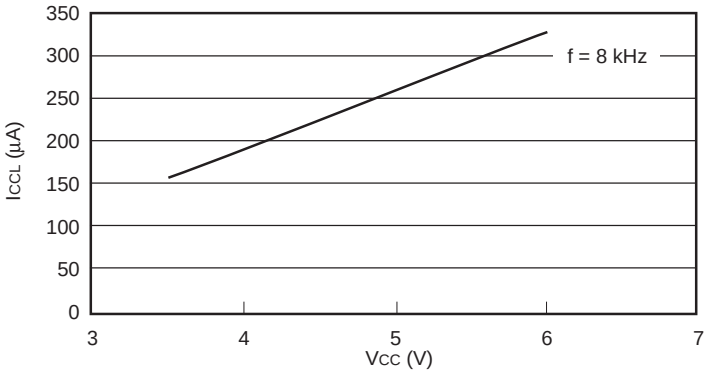
$I_{CCS} - V_{CC}$

T_A = +25 °C, In external clock operation
f = Internal operating frequency



$I_{CCL} - V_{CC}$

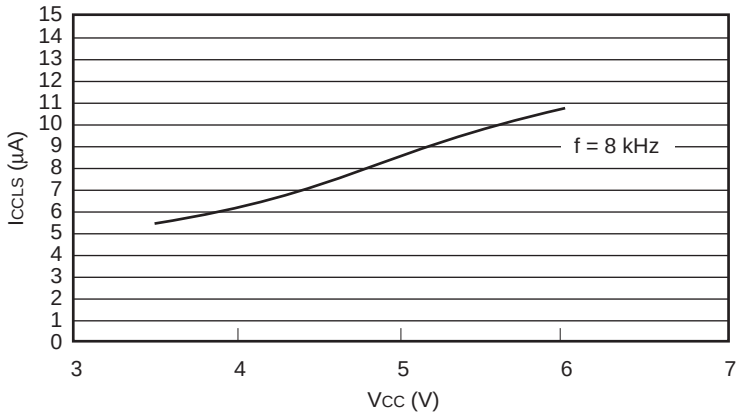
T_A = +25 °C, In external clock operation
f = Internal operating frequency



(Continued)

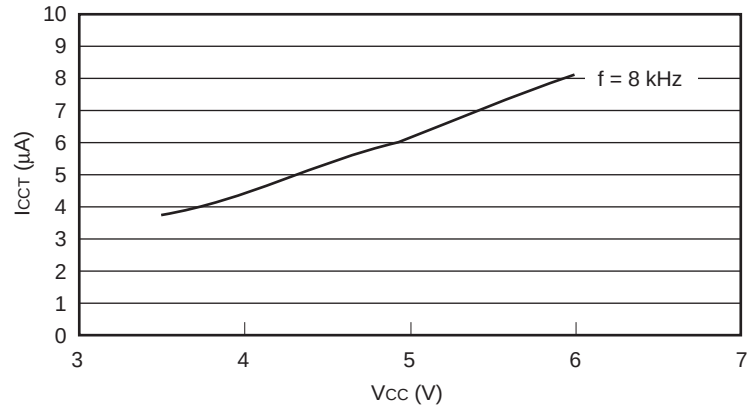
I_{CCLS} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



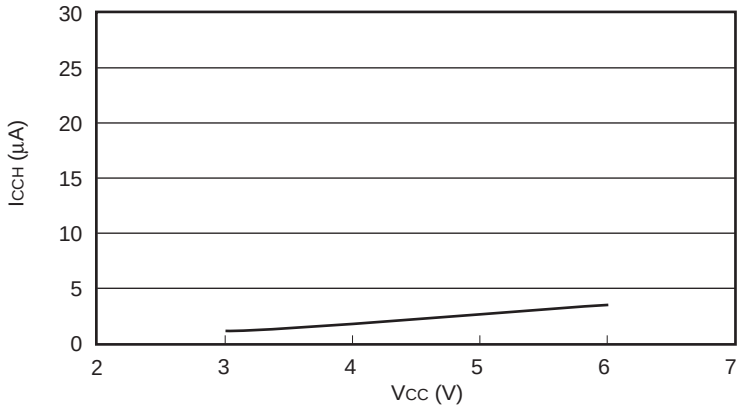
I_{CCT} – V_{CC}

T_A = +25 °C, In external clock operation
f = Internal operating frequency



I_{CCH} – V_{CC}

Stopping, T_A = +25 °C

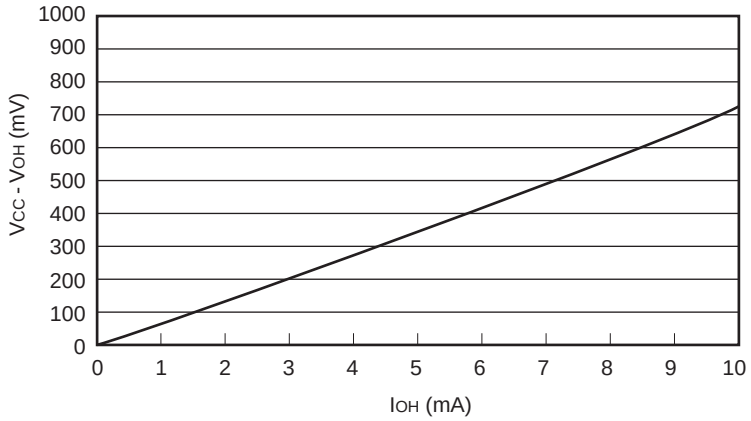


(Continued)

(Continued)

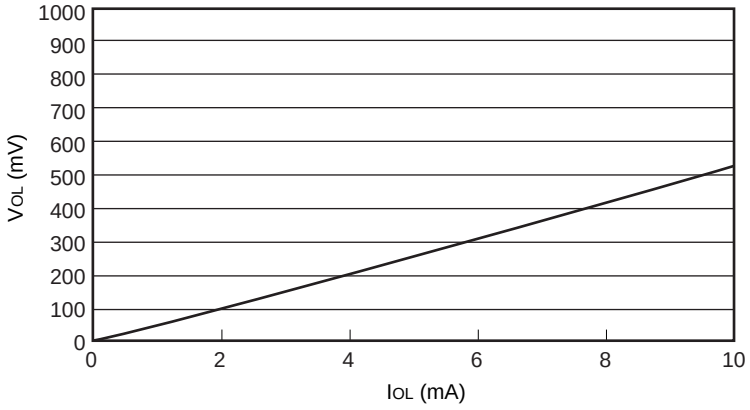
$(V_{CC} - V_{OH})$ – I_{OH}

T_A = +25 °C, V_{CC} = 4.5 V



V_{OL} – I_{OL}

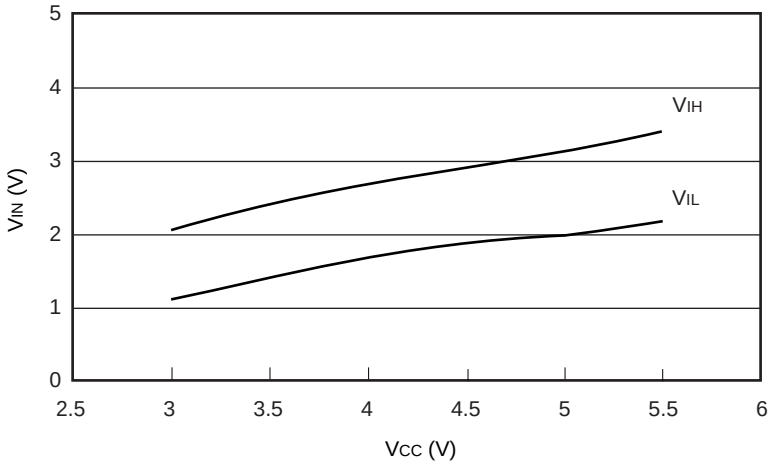
T_A = +25 °C, V_{CC} = 4.5 V



“H” level input voltage/ “L” level input voltage

V_{IN} – V_{CC}

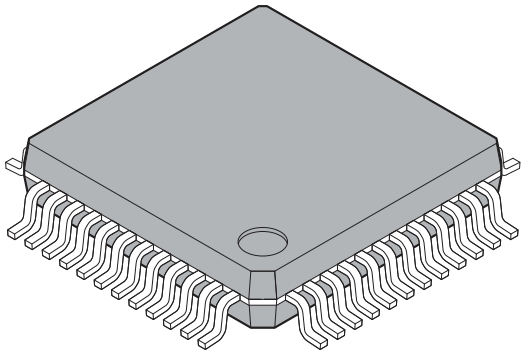
T_A = +25 °C



■ ORDERING INFORMATION

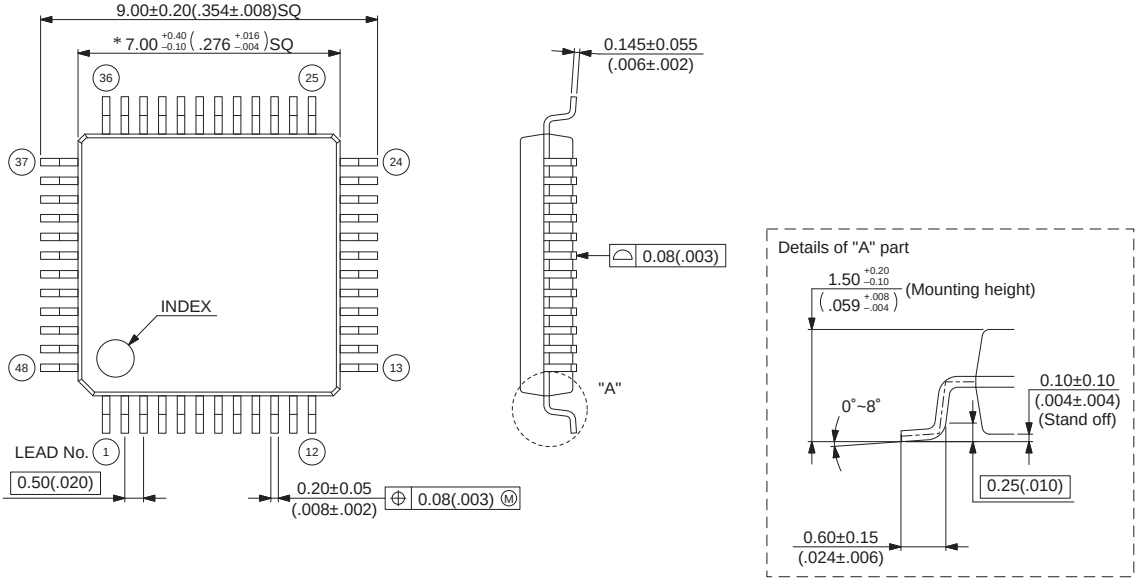
Part number	Package	Remarks
MB90F897PMT MB90F897SPMT MB90F897YPMT MB90F897YSPMT	48-pin plastic LQFP (FPT-48P-M26)	

■ PACKAGE DIMENTION

48-pin plastic LQFP		
	Lead pitch	0.50 mm
	Package width × package length	7 × 7 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.17 g
(FPT-48P-M26)	Code (Reference)	P-LFQFP48-7×7-0.50

48-pin plastic LQFP
(FPT-48P-M26)

Note 1) * : These dimensions include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Added the following part numbers under development. MB90F897Y, MB90F897YS
1	■ FEATURES	Added as follows. • Models that support + 150 °C (MB90F897Y/YS)
8	■ PIN DESCRIPTION	Corrected the function of pin SCK0 on pin number 43. UART1 → UART0
11	■ HANDLING DEVICES	Corrected the description for "• Handling Unused Pins". unused input pins → unused I/O pins
12		"• Support for + 125 °C" → "• Support for + 125 °C / + 150 °C"
13	■ BLOCK DIAGRAM	Corrected the arrow for "pin X0 and X1" in the clock control circuit. "input → "→ "input/output←→"
		Corrected the arrow for "pin TIN0 and pin TIN1" in 16-bit reload timer (2ch). "output →" →" input←"
23	■ INTERRUPT SOURCES, INTERRUPT VECTORS, AND INTERRUPT CONTROL REGISTERS	Corrected footnotes in the address column for ICR05 and ICR07 of the interrupt control register. $0000B5_H$*2 → $0000B5_H$*1 $10000B7_H$*1 → $0000B7_H$*2
24		Corrected the description for footnote *2. 16-bit reload timer → Input capture 1
—	■ PERIPHERAL RESOURCES	Deleted the section Refer to the hardware manual, for details of peripheral resources.
25	■ FLASH MEMORY CONFIGURATION	Changed the item name from "PERIPHERAL RESOURCES" to "FLASH MEMORY CONFIGURATION".
26	■ ELECTRIC CHARACTERISTICS 1. Absolute Maximum Rating	Item: Added the rating value for MB90F897Y/YS to the operating temperature. Min: – 40 °C, Max: + 150 °C
27		Added footnote*9.
28	2. Recommended Operating Conditions	Item: Added the rating value for MB90F897Y/YS to the operating temperature. Min: – 40 °C,Max: + 150 °C
		Added footnote *3.
31, 32	3. DC Characteristics	Added DC characteristics for "MB90F897Y/YS".
33 to 40	4. AC Characteristics 5. A/D converter	Changed the condition description in the upper right of the table. T_A = – 40 °C to +125 °C → T_A = – 40 °C to +125 °C/ + 150 °C (Only MB90F897Y/YS)
49	■ ORDERING INFORMATION	Added the following part numbers. MB90F897YPMT, MB90F897YSPMT

The vertical lines marked in the left side of the page show the changes.

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3329
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

Edited: Sales Promotion Department