512K × 4 BANKS × 32BITS SDRAM

Table of Contents-

1. GENERAL DESCRIPTION

W9864G2JH is a high-speed synchronous dynamic random access memory (SDRAM), organized as 512K words × 4 banks × 32 bits. W9864G2JH delivers a data bandwidth of up to 200M words per second. For different application, W9864G2JH is sorted into the following speed grades: -5, -6, -6I, -6A, -6K and -7. The -5 parts can run up to 200MHz/CL3. The -6, -6I, -6A and -6K parts can run up to 166 MHz/CL3, -6I industrial grade, -6A automotive grade which is guaranteed to support -40°C ≤ T_A ≤ 85°C. If -6K automotive grade offered, has two simultaneous requirements: ambient temperature (T_A) surrounding the device cannot be less than -40°C or greater than +105°C, and the case temperature (T_{CASE}) cannot be less than -40°C or greater than +105°C.) The -7 parts can run up to 143 MHz/CL3.

Accesses to the SDRAM are burst oriented. Consecutive memory location in one page can be accessed at a burst length of 1, 2, 4, 8 or full page when a bank and row is selected by an ACTIVE command. Column addresses are automatically generated by the SDRAM internal counter in burst operation. Random column read is also possible by providing its address at each clock cycle. The multiple bank nature enables interleaving among internal banks to hide the precharging time.

By having a programmable Mode Register, the system can change burst length, latency cycle, interleave or sequential burst to maximize its performance. W9864G2JH is ideal for main memory in high performance applications.

2. FEATURES

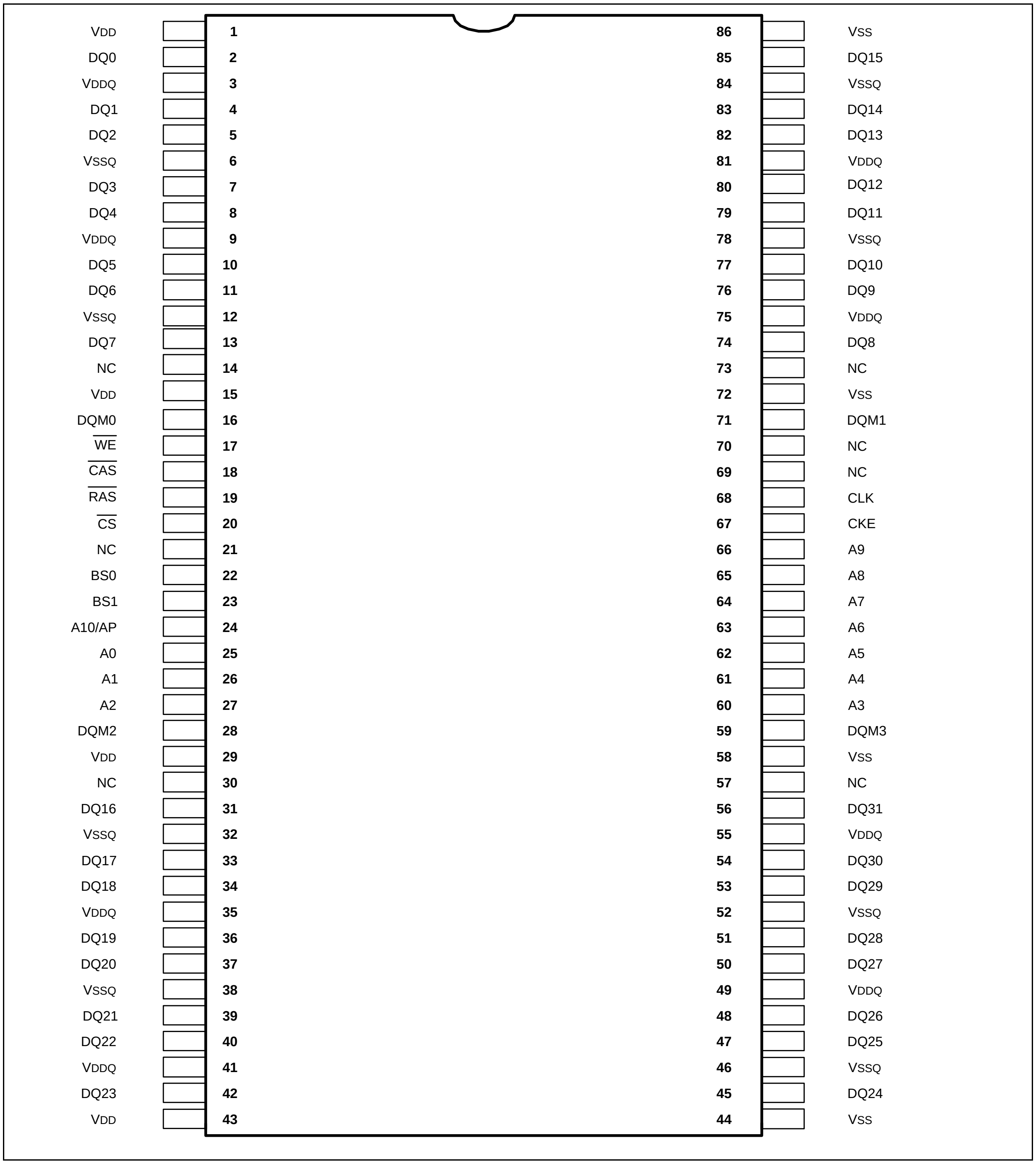
- 3.3V ± 0.3V for -5/-6/-6I/-6A/-6K grades power supply
  2.7V~3.6V for -7 grade power supply
- Up to 200 MHz Clock Frequency
- 524,288 words × 4 banks × 32 bits organization
- Self Refresh Current: Standard and Low Power
- CAS Latency: 2 & 3
- Burst Length: 1, 2, 4, 8 and full page
- Sequential and Interleave Burst
- Byte data controlled by DQM0-3
- Auto-precharge and controlled precharge
- Burst read, single write operation
- 4K Refresh cycles/64 mS, @ -40°C ≤ T_A / T_{CASE} ≤ 85°C
- 4K Refresh cycles/16 mS, @ 85°C < T_A / T_{CASE} ≤ 105°C
- Interface: LVTTL
- Packaged in TSOP II 86-pin, using Lead free materials with RoHS compliant

*** Note:** Not support self refresh function with T_A / T_{CASE} > 85°C

3. ORDER INFORMATION

PART NUMBER	SPEED	MAXIMUM SELF REFRESH CURRENT	OPERATING TEMPERATURE
W9864G2JH-5	200MHz/CL3	2mA	0°C ~ 70°C
W9864G2JH-6	166MHz/CL3	2mA	0°C ~ 70°C
W9864G2JH-6I	166MHz/CL3	2mA	-40°C ~ 85°C
W9864G2JH-6A	166MHz/CL3	2mA	-40°C ~ 85°C
W9864G2JH-6K	166MHz/CL3	5mA	-40°C ~ 105°C
W9864G2JH-7	143MHz/CL3	2mA	0°C ~ 70°C

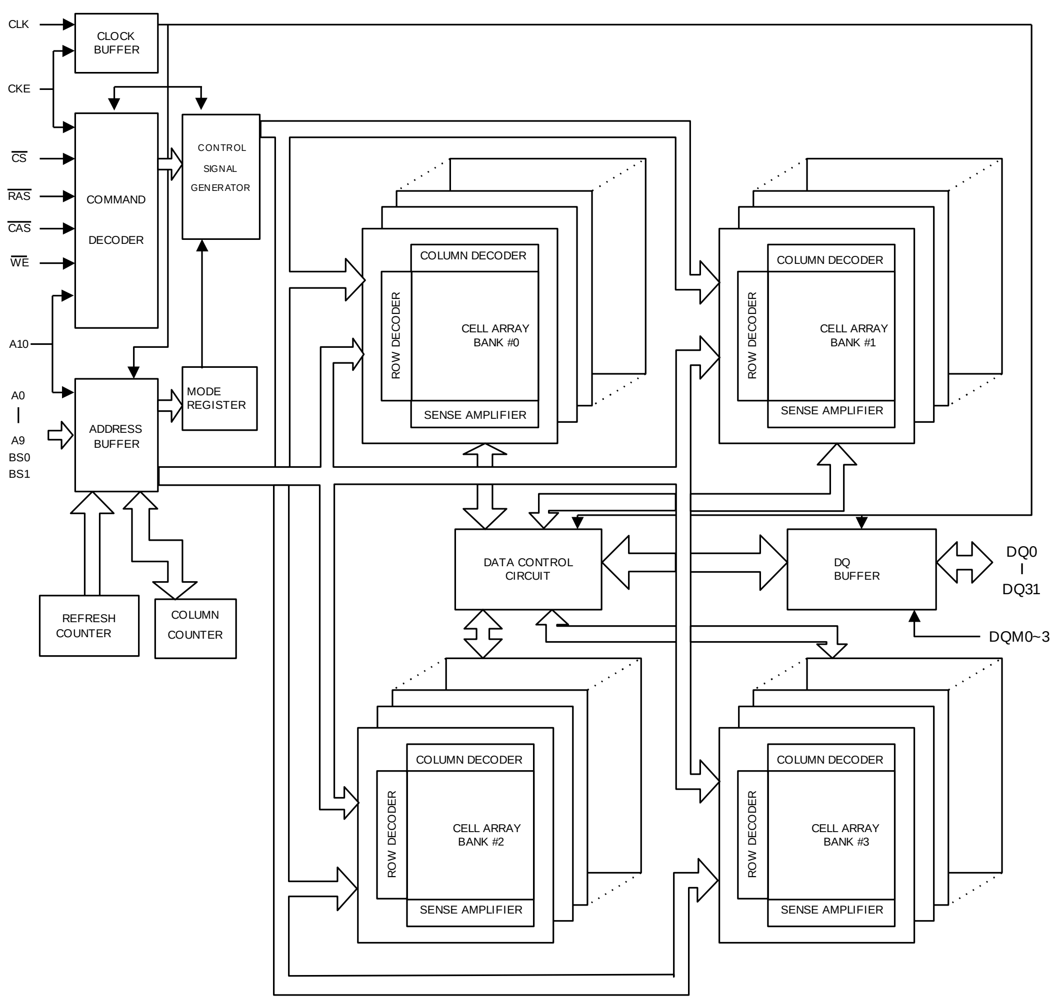
4. PIN CONFIGURATION



5. PIN DESCRIPTION

PIN NUMBER	PIN NAME	FUNCTION	DESCRIPTION
24, 25, 26, 27, 60, 61, 62, 63, 64, 65, 66	A0–A10	Address	Multiplexed pins for row and column address. Row address: A0–A10. Column address: A0–A7. A10 is sampled during a precharge command to determine if all banks are to be precharged or bank selected by BS0, BS1.
22, 23	BS0, BS1	Bank Select	Select bank to activate during row address latch time, or bank to read/write during address latch time.
2, 4, 5, 7, 8, 10, 11, 13, 31, 33, 34, 36, 37, 39, 40, 42, 45, 47, 48, 50, 51, 53, 54, 56, 74, 76, 77, 79, 80, 82, 83, 85	DQ0–DQ31	Data Input/ Output	Multiplexed pins for data output and input.
20	$\overline{CS}$	Chip Select	Disable or enable the command decoder. When command decoder is disabled, new command is ignored and previous operation continues.
19	$\overline{RAS}$	Row Address Strobe	Command input. When sampled at the rising edge of the clock $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ define the operation to be executed.
18	$\overline{CAS}$	Column Address Strobe	Referred to $\overline{RAS}$
17	$\overline{WE}$	Write Enable	Referred to $\overline{RAS}$
16, 28, 59, 71	DQM0–DQM3	Input/Output Mask	The output buffer is placed at Hi-Z (with latency of 2) when DQM is sampled high in read cycle. In write cycle, sampling DQM high will block the write operation with zero latency.
68	CLK	Clock Inputs	System clock used to sample inputs on the rising edge of clock.
67	CKE	Clock Enable	CKE controls the clock activation and deactivation. When CKE is low, Power Down mode, Suspend mode, or Self Refresh mode is entered.
1, 15, 29, 43	VDD	Power	Power for input buffers and logic circuit inside DRAM.
44, 58, 72, 86	VSS	Ground	Ground for input buffers and logic circuit inside DRAM.
3, 9, 35, 41, 49, 55, 75, 81	VDDQ	Power for I/O Buffer	Separated power from VDD, to improve DQ noise immunity.
6, 12, 32, 38, 46, 52, 78, 84	VSSQ	Ground for I/O Buffer	Separated ground from VSS, to improve DQ noise immunity.
14, 21, 30, 57, 69, 70, 73	NC	No Connection	No connection.

6. BLOCK DIAGRAM



NOTE:
The cell array configuration is 2048 * 256 * 32

7. FUNCTIONAL DESCRIPTION

7.1 Power Up and Initialization

The default power up state of the mode register is unspecified. The following power up and initialization sequence need to be followed to guarantee the device being preconditioned to each user specific needs.

During power up, all V_{DD} and V_{DDQ} pins must be ramp up simultaneously to the specified voltage when the input signals are held in the "NOP" state. The power up voltage must not exceed V_{DD} + 0.3V on any of the input pins or V_{DD} supplies. After power up, an initial pause of 200 µS is required followed by a precharge of all banks using the precharge command. To prevent data contention on the DQ bus during power up, it is required that the DQM and CKE pins be held high during the initial pause period. Once all banks have been precharged, the Mode Register Set Command must be issued to initialize the Mode Register. An additional eight Auto Refresh cycles (CBR) are also required before or after programming the Mode Register to ensure proper subsequent operation.

7.2 Programming Mode Register

After initial power up, the Mode Register Set Command must be issued for proper device operation. All banks must be in a precharged state and CKE must be high at least one cycle before the Mode Register Set Command can be issued. The Mode Register Set Command is activated by the low signals of $\overline{RAS}$, $\overline{CAS}$, $\overline{CS}$ and $\overline{WE}$ at the positive edge of the clock. The address input data during this cycle defines the parameters to be set as shown in the Mode Register Operation table. A new command may be issued following the mode register set command once a delay equal to t_{RSC} has elapsed. Please refer to the next page for Mode Register Set Cycle and Operation Table.

7.3 Bank Activate Command

The Bank Activate command must be applied before any Read or Write operation can be executed. The operation is similar to RAS activate in EDO DRAM. The delay from when the Bank Activate command is applied to when the first read or write operation can begin must not be less than the RAS to CAS delay time (t_{RCD}). Once a bank has been activated it must be precharged before another Bank Activate command can be issued to the same bank. The minimum time interval between successive Bank Activate commands to the same bank is determined by the RAS cycle time of the device (t_{RC}). The minimum time interval between interleaved Bank Activate commands (Bank A to Bank B and vice versa) is the Bank to Bank delay time (t_{RRD}). The maximum time that each bank can be held active is specified as t_{RAS} (max.).

7.4 Read and Write Access Modes

After a bank has been activated, a read or write cycle can be followed. This is accomplished by setting $\overline{RAS}$ high and $\overline{CAS}$ low at the clock rising edge after minimum of t_{RCD} delay. $\overline{WE}$ pin voltage level defines whether the access cycle is a read operation ($\overline{WE}$ high), or a write operation ($\overline{WE}$ low). The address inputs determine the starting column address. Reading or writing to a different row within an activated bank requires the bank be precharged and a new Bank Activate command be issued. When more than one bank is activated, interleaved bank Read or Write operations are possible. By using the programmed burst length and alternating the access and precharge operations between multiple banks, seamless data access operation among many different pages can be realized. Read or Write Commands can also be issued to the same bank or between active banks on every clock cycle.

7.5 Burst Read Command

The Burst Read command is initiated by applying logic low level to $\overline{CS}$ and $\overline{CAS}$ while holding $\overline{RAS}$ and $\overline{WE}$ high at the rising edge of the clock. The address inputs determine the starting column address for the burst. The Mode Register sets type of burst (sequential or interleave) and the burst length (1, 2, 4, 8 and full page) during the Mode Register Set Up cycle. Table 2 and 3 in the next page explain the address sequence of interleave mode and sequence mode.

7.6 Burst Command

The Burst Write command is initiated by applying logic low level to $\overline{CS}$, $\overline{CAS}$ and $\overline{WE}$ while holding $\overline{RAS}$ high at the rising edge of the clock. The address inputs determine the starting column address. Data for the first burst write cycle must be applied on the DQ pins on the same clock cycle that the Write Command is issued. The remaining data inputs must be supplied on each subsequent rising clock edge until the burst length is completed. Data supplied to the DQ pins after burst finishes will be ignored.

7.7 Read Interrupted by a Read

A Burst Read may be interrupted by another Read Command. When the previous burst is interrupted, the remaining addresses are overridden by the new read address with the full burst length. The data from the first Read Command continues to appear on the outputs until the CAS Latency from the interrupting Read Command the is satisfied.

7.8 Read Interrupted by a Write

To interrupt a burst read with a Write Command, DQM may be needed to place the DQs (output drivers) in a high impedance state to avoid data contention on the DQ bus. If a Read Command will issue data on the first and second clocks cycles of the write operation, DQM is needed to insure the DQs are tri-stated. After that point the Write Command will have control of the DQ bus and DQM masking is no longer needed.

7.9 Write Interrupted by a Write

A burst write may be interrupted before completion of the burst by another Write Command. When the previous burst is interrupted, the remaining addresses are overridden by the new address and data will be written into the device until the programmed burst length is satisfied.

7.10 Write Interrupted by a Read

A Read Command will interrupt a burst write operation on the same clock cycle that the Read Command is activated. The DQs must be in the high impedance state at least one cycle before the new read data appears on the outputs to avoid data contention. When the Read Command is activated, any residual data from the burst write cycle will be ignored.

7.11 Burst Stop Command

A Burst Stop Command may be used to terminate the existing burst operation but leave the bank open for future Read or Write Commands to the same page of the active bank, if the burst length is full page. Use of the Burst Stop Command during other burst length operations is illegal. The Burst Stop Command is defined by having $\overline{RAS}$ and $\overline{CAS}$ high with $\overline{CS}$ and $\overline{WE}$ low at the rising edge of the clock. The data DQs go to a high impedance state after a delay, which is equal to the CAS Latency in a burst read cycle, interrupted by Burst Stop.

7.12 Addressing Sequence of Sequential Mode

A column access is performed by increasing the address from the column address which is input to the device. The disturb address is varied by the Burst Length as shown in Table 2.

Table 2 Address Sequence of Sequential Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	n	BL = 2 (disturb address is A0)
Data 1	n + 1	No address carry from A0 to A1
Data 2	n + 2	BL = 4 (disturb addresses are A0 and A1)
Data 3	n + 3	No address carry from A1 to A2
Data 4	n + 4	
Data 5	n + 5	BL = 8 (disturb addresses are A0, A1 and A2)
Data 6	n + 6	No address carry from A2 to A3
Data 7	n + 7	

7.13 Addressing Sequence of Interleave Mode

A column access is started in the input column address and is performed by inverting the address bit in the sequence shown in Table 3.

Table 3 Address Sequence of Interleave Mode

DATA	ACCESS ADDRESS	BURST LENGTH
Data 0	A8 A7 A6 A5 A4 A3 A2 A1 A0	BL = 2
Data 1	A8 A7 A6 A5 A4 A3 A2 A1 $\overline{A0}$	
Data 2	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ A0	BL = 4
Data 3	A8 A7 A6 A5 A4 A3 A2 $\overline{A1}$ $\overline{A0}$	
Data 4	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 A0	BL = 8
Data 5	A8 A7 A6 A5 A4 A3 $\overline{A2}$ A1 $\overline{A0}$	
Data 6	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ A0	
Data 7	A8 A7 A6 A5 A4 A3 $\overline{A2}$ $\overline{A1}$ $\overline{A0}$	

7.14 Auto-precharge Command

If A10 is set to high when the Read or Write Command is issued, then the Auto-precharge function is entered. During Auto-precharge, a Read Command will execute as normal with the exception that the active bank will begin to precharge automatically before all burst read cycles have been completed. Regardless of burst length, it will begin a certain number of clocks prior to the end of the scheduled burst cycle. The number of clocks is determined by CAS Latency.

A Read or Write Command with Auto-precharge cannot be interrupted before the entire burst operation is completed for the same bank. Therefore, use of a Read, Write, or Precharge Command is prohibited during a read or write cycle with Auto-precharge. Once the precharge operation has started, the bank cannot be reactivated until the Precharge time (t_{RP}) has been satisfied. Issue of Auto-precharge command is illegal if the burst is set to full page length. If A10 is high when a Write Command is issued, the Write with Auto-precharge function is initiated. The SDRAM automatically enters the precharge operation two clocks delay from the last burst write cycle. This delay is referred to as write t_{WR}. The bank undergoing Auto-precharge cannot be reactivated until t_{WR} and t_{RP} are satisfied. This is referred to as t_{DAL}, Data-in to Active delay ($t_{DAL} = t_{WR} + t_{RP}$). When using the Auto-precharge Command, the interval between the Bank Activate Command and the beginning of the internal precharge operation must satisfy t_{RAS} (min).

7.15 Precharge Command

The Precharge Command is used to precharge or close a bank that has been activated. The Precharge Command is entered when $\overline{CS}$, $\overline{RAS}$ and $\overline{WE}$ are low and $\overline{CAS}$ is high at the rising edge of the clock. The Precharge Command can be used to precharge each bank separately or all banks simultaneously. Three address bits, A10, BS0 and BS1 are used to define which bank(s) is to be precharged when the command is issued. After the Precharge Command is issued, the precharged bank must be reactivated before a new read or write access can be executed. The delay between the Precharge Command and the Activate Command must be greater than or equal to the Precharge time (t_{RP}).

7.16 Self Refresh Command

The Self Refresh Command is defined by having $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and CKE held low with $\overline{WE}$ high at the rising edge of the clock. All banks must be idle prior to issuing the Self Refresh Command. Once the command is registered, CKE must be held low to keep the device in Self Refresh mode. When the SDRAM has entered Self Refresh mode all of the external control signals, except CKE, are disabled. The clock is internally disabled during Self Refresh Operation to save power. The device will exit Self Refresh operation after CKE is returned high. Any subsequent commands can be issued after t_{XSR} from the end of Self Refresh Command.

If, during normal operation, AUTO REFRESH cycles are issued in bursts (as opposed to being evenly distributed), a burst of 4,096 AUTO REFRESH cycles should be completed just prior to entering and just after exiting the self refresh mode.

7.17 Power Down Mode

The Power Down mode is initiated by holding CKE low. All of the receiver circuits except CKE are gated off to reduce the power. The Power Down mode does not perform any refresh operations, therefore the device can not remain in Power Down mode longer than the Refresh period (t_{REF}) of the device.

The Power Down mode is exited by bringing CKE high. When CKE goes high, a No Operation Command is required on the next rising clock edge, depending on t_{CK}. The input buffers need to be enabled with CKE held high for a period equal to t_{CKS} (min.) + t_{CK} (min.).

7.18 No Operation Command

The No Operation Command should be used in cases when the SDRAM is in a idle or a wait state to prevent the SDRAM from registering any unwanted commands between operations. A No Operation Command is registered when $\overline{CS}$ is low with $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ held high at the rising edge of the clock. A No Operation Command will not terminate a previous operation that is still executing, such as a burst read or write cycle.

7.19 Deselect Command

The Deselect Command performs the same function as a No Operation Command. Deselect Command occurs when $\overline{CS}$ is brought high, the $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ signals become don’t cares.

7.20 Clock Suspend Mode

During normal access mode, CKE must be held high enabling the clock. When CKE is registered low while at least one of the banks is active, Clock Suspend Mode is entered. The Clock Suspend mode deactivates the internal clock and suspends any clocked operation that was currently being executed. There is a one clock delay between the registration of CKE low and the time at which the SDRAM operation suspends. While in Clock Suspend mode, the SDRAM ignores any new commands that are issued. The Clock Suspend mode is exited by bringing CKE high. There is a one clock cycle delay from when CKE returns high to when Clock Suspend mode is exited.

8. OPERATION MODE

Fully synchronous operations are performed to latch the commands at the positive edges of CLK. Table 1 shows the truth table for the operation commands.

TABLE 1 TRUTH TABLE (NOTE (1), (2))

COMMAND	Device State	CKEn-1	CKEn	DQM	BS0, 1	A10	A0-A9	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$
Bank Active	Idle	H	x	x	v	v	V	L	L	H	H
Bank Precharge	Any	H	x	x	v	L	x	L	L	H	L
Precharge All	Any	H	x	x	x	H	x	L	L	H	L
Write	Active (3)	H	x	x	v	L	v	L	H	L	L
Write with Auto-precharge	Active (3)	H	x	x	v	H	v	L	H	L	L
Read	Active (3)	H	x	x	v	L	v	L	H	L	H
Read with Auto-precharge	Active (3)	H	x	x	v	H	v	L	H	L	H
Mode Register Set	Idle	H	x	x	v	v	v	L	L	L	L
No-Operation	Any	H	x	x	x	x	x	L	H	H	H
Burst Stop	Active (4)	H	x	x	x	x	x	L	H	H	L
Device Deselect	Any	H	x	x	x	x	x	H	x	x	x
Auto-Refresh	Idle	H	H	x	x	x	x	L	L	L	H
Self-Refresh Entry	Idle	H	L	x	x	x	x	L	L	L	H
Self Refresh Exit	idle (S.R)	L L	H H	x x	x x	x x	x x	H L	x H	x H	x x
Clock suspend Mode Entry	Active	H	L	x	x	x	x	x	x	x	x
Power Down Mode Entry	Idle Active (5)	H H	L L	x x	x x	x x	x x	H L	x H	x H	X H
Clock Suspend Mode Exit	Active	L	H	x	x	x	x	x	x	x	X
Power Down Mode Exit	Any (power down)	L L	H H	x x	x x	x x	x x	H L	x H	x H	X H
Data write/Output Enable	Active	H	x	L	x	x	x	x	x	x	x
Data Write/Output Disable	Active	H	x	H	x	x	x	x	x	x	x

Notes:

(1) v = valid, x = Don't care, L = Low Level, H = High Level

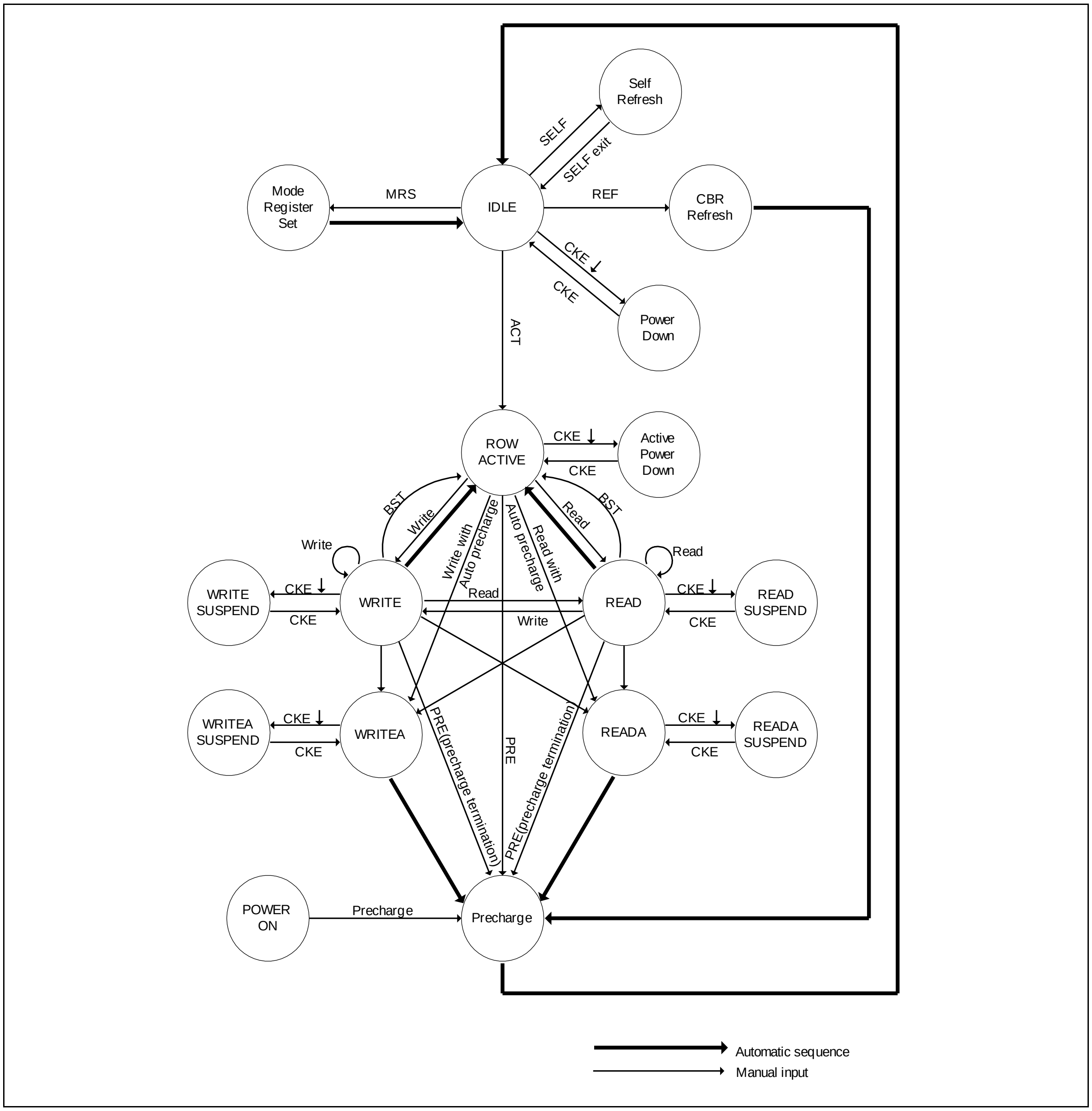
(2) CKEn signal is input leve l when commands are provided.

(3) These are state of bank designated by BS0, BS1 signals.

(4) Device state is full page burst operation.

(5) Power Down Mode can not be entered in the burst cycle.
When this command asserts in the burst cycle, device state is clock suspend mode.

8.1 Simplified Stated Diagram



MRS = Mode Register Set

REF = Refresh

ACT = Active

PRE = Precharge

WRITEA = Write with Auto-precharge

READA = Read with Auto-precharge

9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum Ratings

PARAMETER	SYMBOL	RATING	UNIT	NOTES
Voltage on any pin relative to VSS	VIN, VOUT	-0.5 ~ VDD + 0.5 (≤ 4.6V max.)	V	1
Voltage on VDD/VDDQ supply relative to VSS	VDD, VDDQ	-0.5 ~ 4.6	V	1
Operating Temperature for -5/-6/-7	TA	0 ~ 70	°C	1, 2
Operating Temperature for -6I/-6A	TA	-40 ~ 85	°C	1, 2
Operating Temperature for -6K	TA	-40 ~ 105	°C	1, 2
Operating Temperature for -6K	TCASE	-40 ~ 105	°C	1, 3, 4, 5, 6
Storage Temperature	TSTG	-55 ~ 150	°C	1
Soldering Temperature (10s)	TSOLDER	260	°C	1
Power Dissipation	PD	1	W	1
Short Circuit Output Current	IOUT	50	mA	1

Notes:

1. Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device
2. Operating ambient temperature is the surrounding temperature of the SDRAM.
3. Operating case temperature is the case surface temperature on the center/top side of the SDRAM
4. Supporting -40°C ≤ TA / TCASE ≤ 85°C with full AC and DC specifications.
5. Supporting -40°C ≤ TA / TCASE ≤ 85°C and being able to extend to 105°C with extend Auto Refresh commands in frequency to a 16 mS period (tREF = 3.9 µS).
6. During operation, the DRAM operation temperature must be maintained between -40 to 105°C for automotive parts under all specification parameters.

9.2 Recommended DC Operating Conditions

PARAMETER	SYM.	MIN.	TYP.	MAX.	UNIT	NOTES
Power Supply Voltage for -5/-6/-6I/-6A/-6K	VDD	3.0	3.3	3.6	V	
Power Supply Voltage (I/O Buffer) for -5/-6/-6I/-6A/-6K	VDDQ	3.0	3.3	3.6	V	
Power Supply Voltage for -7	VDD	2.7	3.3	3.6	V	
Power Supply Voltage (I/O Buffer) for -7	VDDQ	2.7	3.3	3.6	V	
Input High Voltage	VIH	2	-	VDD + 0.3	V	1
Input Low Voltage	VIL	-0.3	-	+0.8	V	2
Output logic high voltage	VOH	2.4	-	-	V	IOH= -2mA
Output logic low voltage	VOL	-	-	0.4	V	IOL= 2mA
Input leakage current	II(L)	-10	-	10	µA	3
Output leakage current	IO(L)	-10	-	10	µA	4

Note:

1. VIH (max.) = VDD/VDDQ+1.5V for pulse width ≤ 5 nS.
2. VIL (min.) = VSS/VSSQ-1.5V for pulse width ≤ 5 nS.
3. Any input 0V ≤ VIN ≤ VDDQ.
   Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.
4. Output disabled, 0V ≤ VOUT ≤ VDDQ

9.3 Capacitance

(V_{DD} = 3.3V ± 0.3V for -5/-6/-6I/-6A/-6K, V_{DD} = 2.7V-3.6V for -7, T_A = 25°C, f = 1 MHz)

PARAMETER	SYM.	MIN.	MAX.	UNIT
Input Capacitance (A0 to A10, BS0, BS1, $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM, CKE)	Ci	2.5	4	pf
Input Capacitance (CLK)	C_{CLK}	2.5	4	pf
Input/Output capacitance (DQ0–DQ31)	Co	4	6.5	pf

Note: These parameters are periodically sampled and not 100% tested

9.4 DC Characteristics

(V_{DD} = 3.3V ± 0.3V for-5/-6, V_{DD} = 2.7V~3.6V for -7 on T_A = 0 to 70°C)
(V_{DD} = 3.3V ± 0.3V for-6I/-6A, T_A = -40 to 85°C)
(V_{DD} = 3.3V ± 0.3V for-6K, T_A / T_{CASE} = -40 to 105°C)

PARAMETER		SYM.	MAX.				UNIT	NOTES
			-5	-6/-6I/-6A	-6K	-7		
Operating Current t_{CK} = min., t_{RC} = min. Active precharge command cycling without burst operation	1 Bank Operation	I_{DD1}	90	80	80	75		3
Standby Current t_{CK} = min., $\overline{CS}$ = V_{IH} $V_{IH/L}$ = V_{IH} (min.)/V_{IL} (max.)	CKE = V_{IH}	I_{DD2}	25	25	25	25		3
Bank: Inactive State	CKE = V_{IL} (Power Down mode)	I_{DD2P}	2	2	5	2		3
Standby Current CLK = V_{IL}, $\overline{CS}$ = V_{IH} $V_{IH/L}$=V_{IH} (min.)/V_{IL} (max.)	CKE = V_{IH}	I_{DD2S}	15	15	15	15		
Bank: Inactive State	CKE = V_{IL} (Power Down mode)	I_{DD2PS}	2	2	5	2	mA	
No Operating Current t_{CK} = min., $\overline{CS}$ = V_{IH} (min.)	CKE = V_{IH}	I_{DD3}	60	55	55	50		
Bank: Active State (4 Banks)	CKE = V_{IL} (Power Down mode)	I_{DD3P}	10	10	12	10		
Burst Operating Current (t_{CK} = min.) Read/Write command cycling		I_{DD4}	145	130	130	120		3, 4
Auto Refresh Current (t_{CK} = min.) Auto refresh command cycling		I_{DD5}	155	140	140	130		3
Self Refresh Current Self refresh mode (CKE = 0.2V)		I_{DD6}	2	2	5	2		

9.5 AC Characteristics and Operating Condition

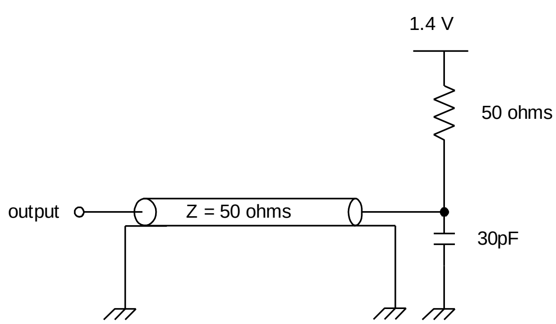
(V_{DD} = 3.3V ± 0.3V for-5/-6, V_{DD} = 2.7V~3.6V for -7 on T_A = 0 to 70°C)
(V_{DD} = 3.3V ± 0.3V for-6I/-6A, T_A = -40 to 85°C)
(V_{DD} = 3.3V ± 0.3V for-6K, T_A / TCASE = -40 to 105°C)(Notes: 5, 6)

PARAMETER		SYM.	-5		-6/-6I/-6A/-6K		-7		UNIT	NOTES
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Ref/Active to Ref/Active Command Period		t_{RC}	55		60		65			
Active to precharge Command Period		t_{RAS}	40	100000	42	100000	45	100000	nS	
Active to Read/Write Command Delay Time		t_{RCD}	15		18		20			
Read/Write(a) to Read/Write(b) Command Period		t_{CCD}	1		1		1		t_{CK}	
Precharge to Active Command Period		t_{RP}	15		18		20		nS	
Active(a) to Active(b) Command Period		t_{RRD}	10		12		14			
Write Recovery Time	CL* = 2	t_{WR}	2		2		2		t_{CK}	
	CL* = 3		2		2		2			
CLK Cycle Time	CL* = 2	t_{CK}	10	1000	7.5	1000	10	1000		
	CL* = 3		5	1000	6	1000	7	1000		
CLK High Level width		t_{CH}	2		2		2			8
CLK Low Level width		t_{CL}	2		2		2			8
Access Time from CLK	CL* = 2	t_{AC}		6		5.5		6		9
	CL* = 3			4.5		5		5.5		
Output Data Hold Time		t_{OH}	3		3		3			9
Output Data High Impedance Time	CL* = 2	t_{HZ}		6		6		6		7
	CL* = 3			4.5		5		5.5		
Output Data Low Impedance Time		t_{LZ}	0		0		0			9
Power Down Mode Entry Time		t_{SB}	0	5	0	6	0	7	nS	
Transition Time of CLK (Rise and Fall)		t_T		1		1		1		
Data-in Set-up Time		t_{DS}	1.5		1.5		1.5			8
Data-in Hold Time		t_{DH}	1.0		1.0		1.0			8
Address Set-up Time		t_{AS}	1.5		1.5		1.5			8
Address Hold Time		t_{AH}	1.0		1.0		1.0			8
CKE Set-up Time		t_{CKS}	1.5		1.5		1.5			8
CKE Hold Time		t_{CKH}	1.0		1.0		1.0			8
Command Set-up Time		t_{CMS}	1.5		1.5		1.5			8
Command Hold Time		t_{CMH}	1.0		1.0		1.0			8
Refresh Time (4K/Refresh Cycles)	-40°C ≤ T_A / TCASE ≤ 85°C	t_{REF}		64		64		64	mS	
	85°C < T_A / TCASE ≤ 105°C	t_{REFA}		--		16		--		
Mode register Set Cycle Time		t_{RSC}	2		2		2		t_{CK}	
Exit self refresh to ACTIVE command		t_{XSR}	70		72		75		nS	

*CL = CAS Latency
* -- = not support

Notes:

1. Operation exceeds "Absolute Maximum Ratings" may cause permanent damage to the devices.
2. All voltages are referenced to V_{SS}.
   - 2.7V~3.6V power supply for -7 speed grades.
3. These parameters depend on the cycle rate and listed values are measured at a cycle rate with the minimum values of t_{CK} and t_{RC}.
4. These parameters depend on the output loading conditions. Specified values are obtained with output open.
5. Power up sequence please refer to "Functional Description" section described before.
6. AC test load diagram.



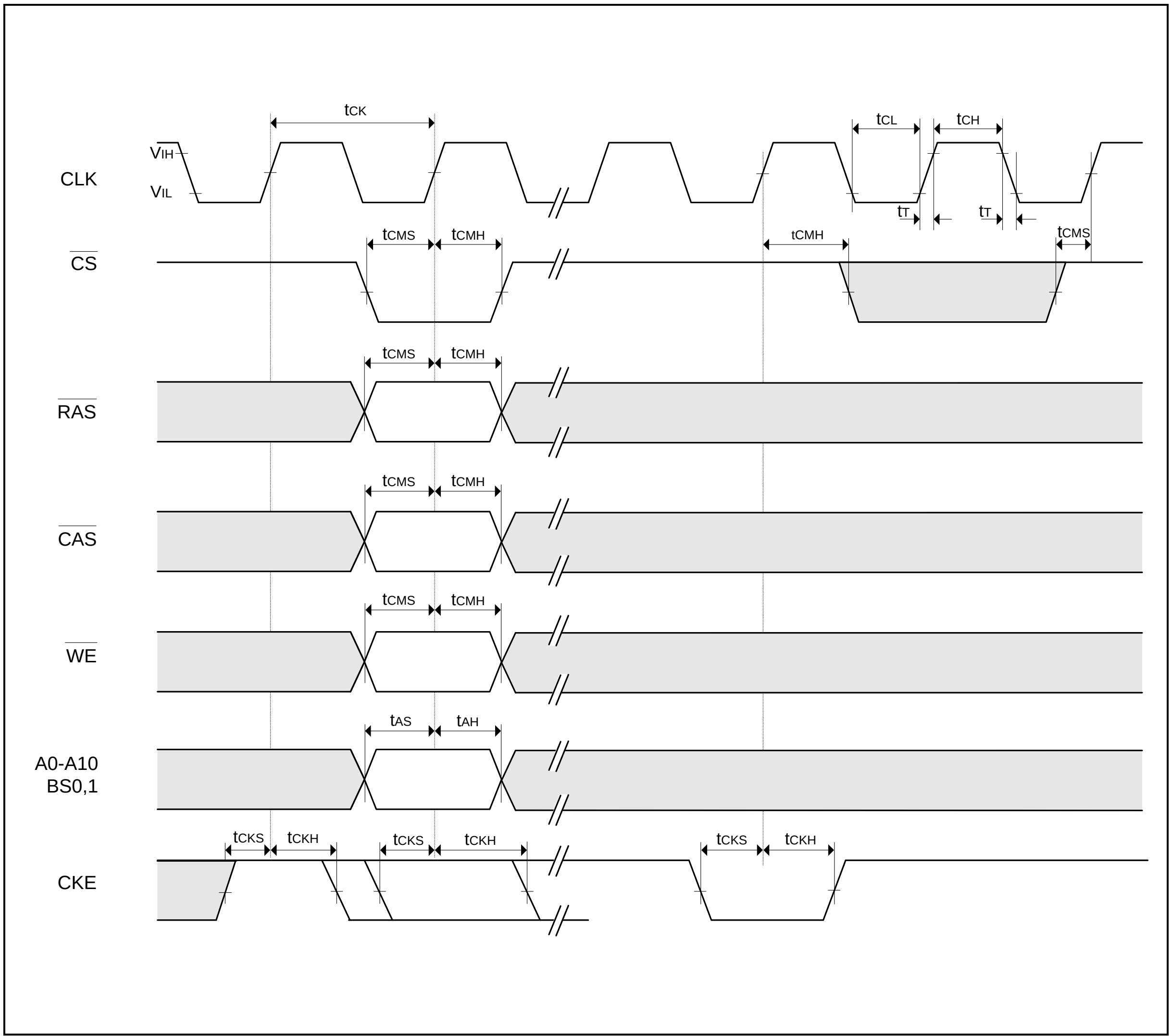
AC TEST LOAD

7. t_{HZ} defines the time at which the outputs achieve the open circuit condition and is not referenced to output level.
8. Assumed input rise and fall time (t_T) = 1nS.

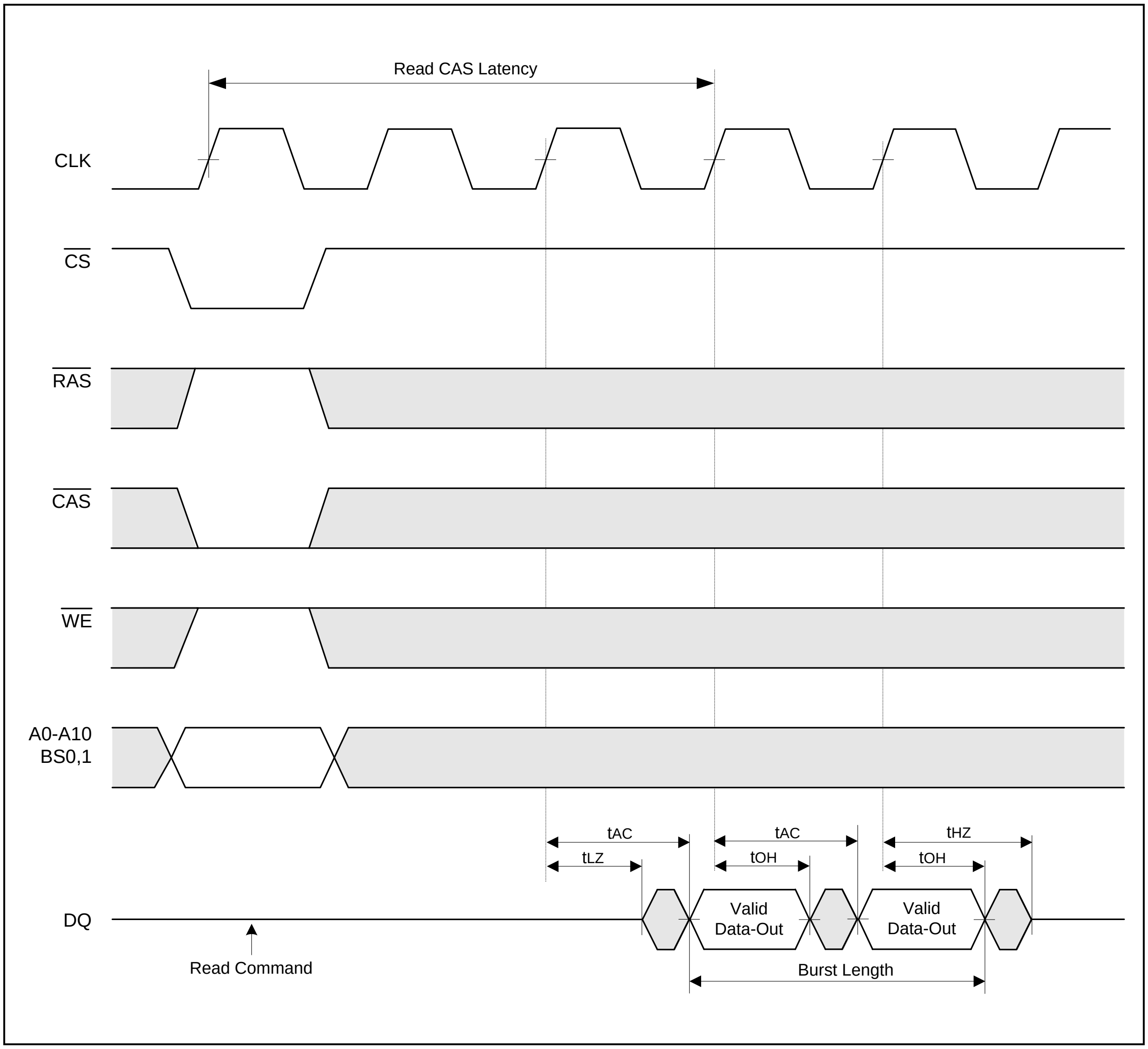
   If tr & tf is longer than 1nS, transient time compensation should be considered,
   i.e., [(tr + tf)/2-1]nS should be added to the parameter.
9. If clock rising time (t_T) is longer than 1nS, (t_T/2-0.5)nS should be added to the parameter.

10. TIMING WAVEFORMS

10.1 Command Input Timing



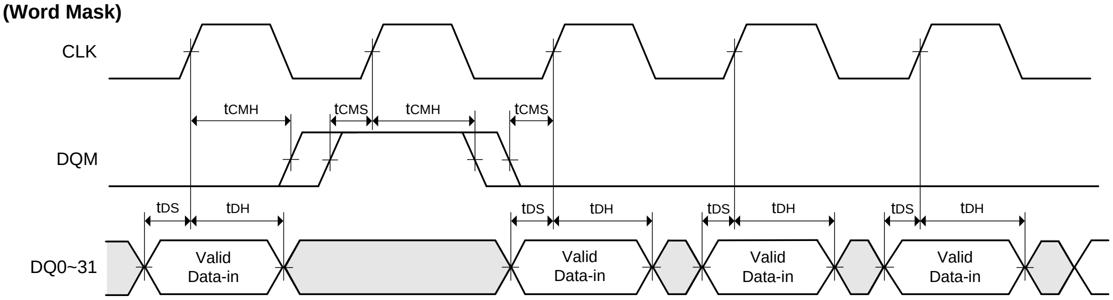
10.2 Read Timing



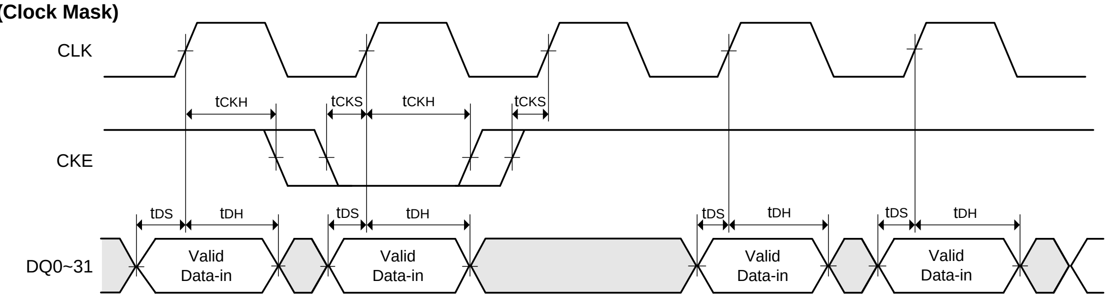
10.3 Control Timing of Input/Output Data

Control Timing of Input Data

(Word Mask)

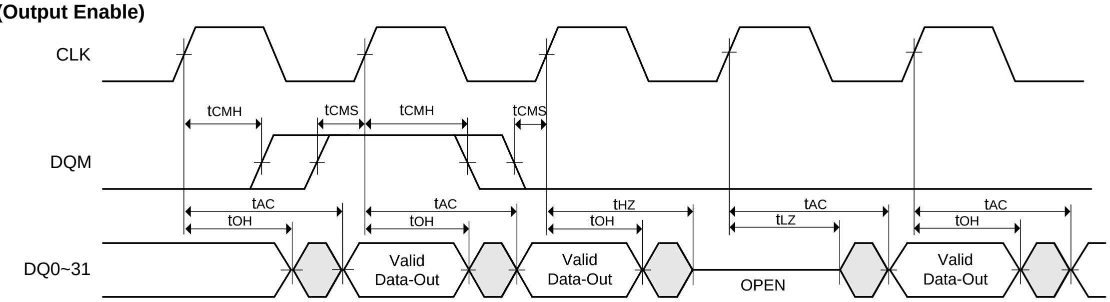


(Clock Mask)

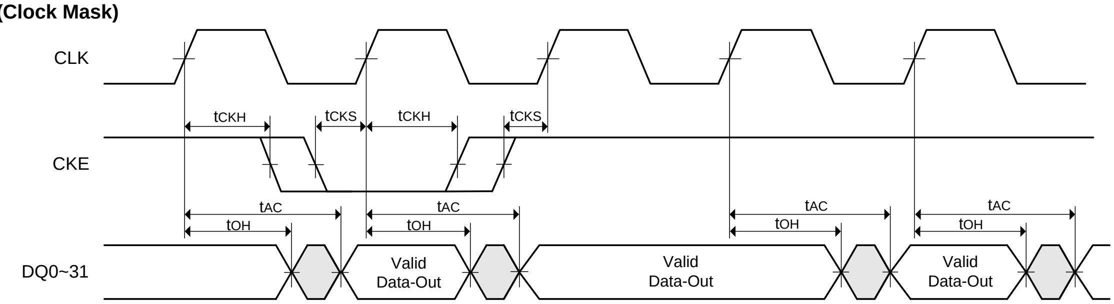


Control Timing of Output Data

(Output Enable)

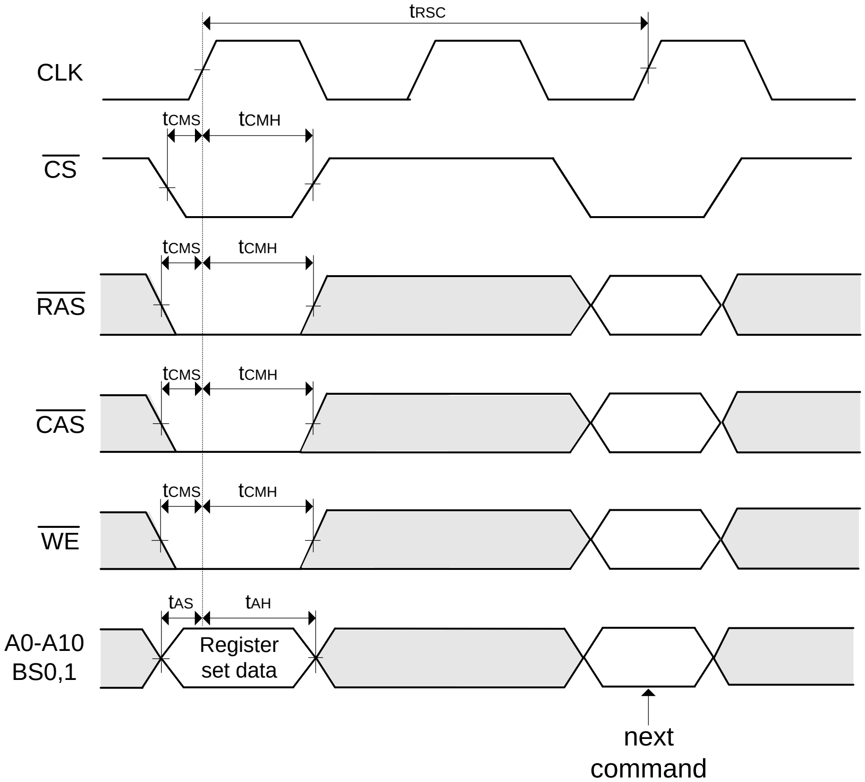


(Clock Mask)



Publication Release Date: Oct. 07, 2013
Revision A02

10.4 Mode Register Set Cycle



A0	Burst Length	
A1		
A2		
A3	Addressing Mode	
A4	CAS Latency	
A5		
A6		
A7	0	(Test Mode)
A8	0	Reserved
A9	Write Mode	
A10	0	Reserved
BS0	0	Mode Register Set
BS1	0	

A2 A1 A0	Burst Length Sequential	Burst Length Interleave
0 0 0	1	1
0 0 1	2	2
0 1 0	4	4
0 1 1	8	8
1 0 0	Reserved	Reserved
1 0 1	Reserved	Reserved
1 1 0	Reserved	Reserved
1 1 1	Full Page	Reserved

A3	Addressing Mode
0	Sequential
1	Interleave

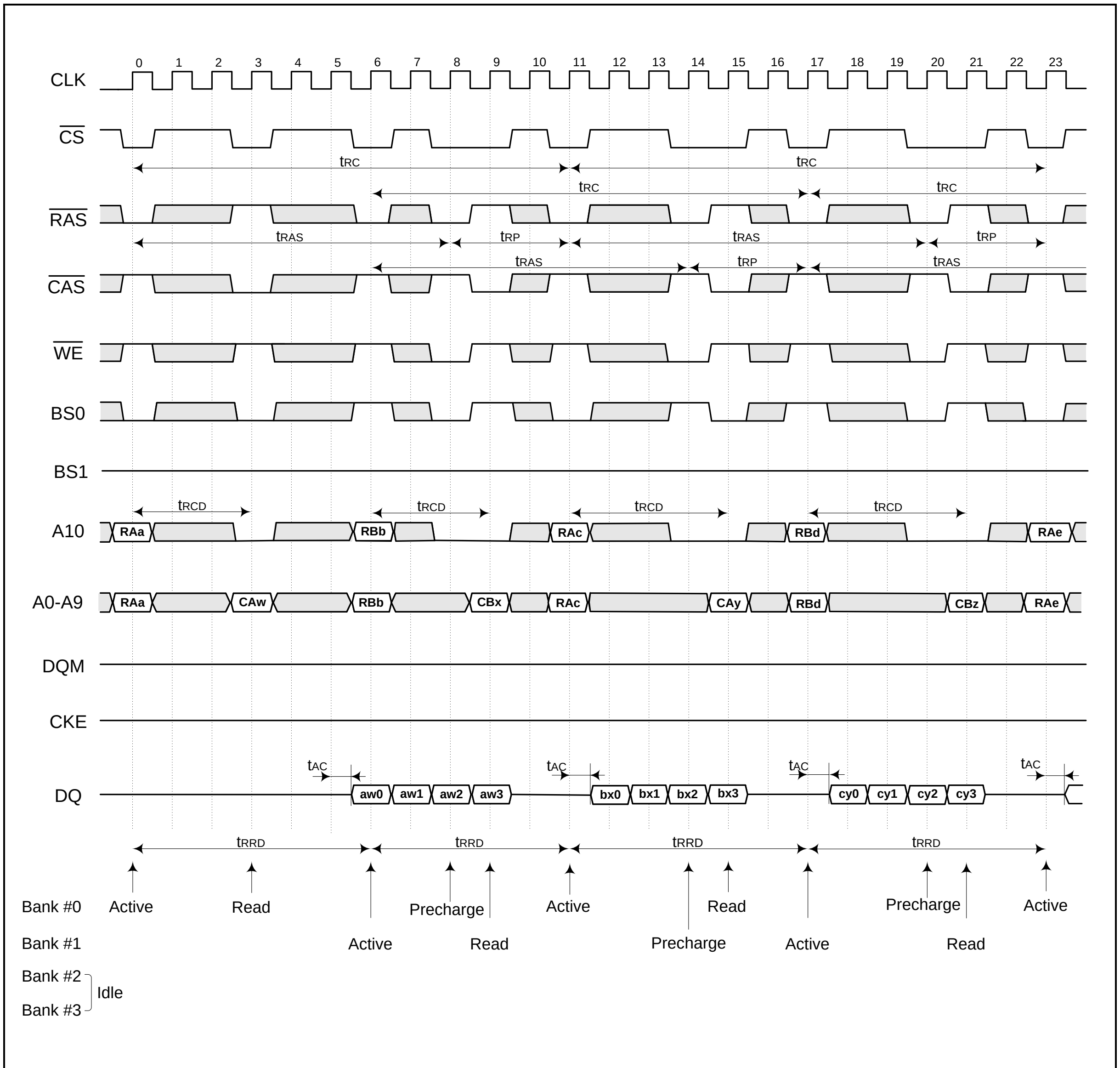
A6 A5 A4	CAS Latency
0 0 0	Reserved
0 0 1	Reserved
0 1 0	2
0 1 1	3
1 0 0	Reserved

A9	Single Write Mode
0	Burst read and Burst write
1	Burst read and single write

* "Reserved" should stay "0" during MRS cycle.

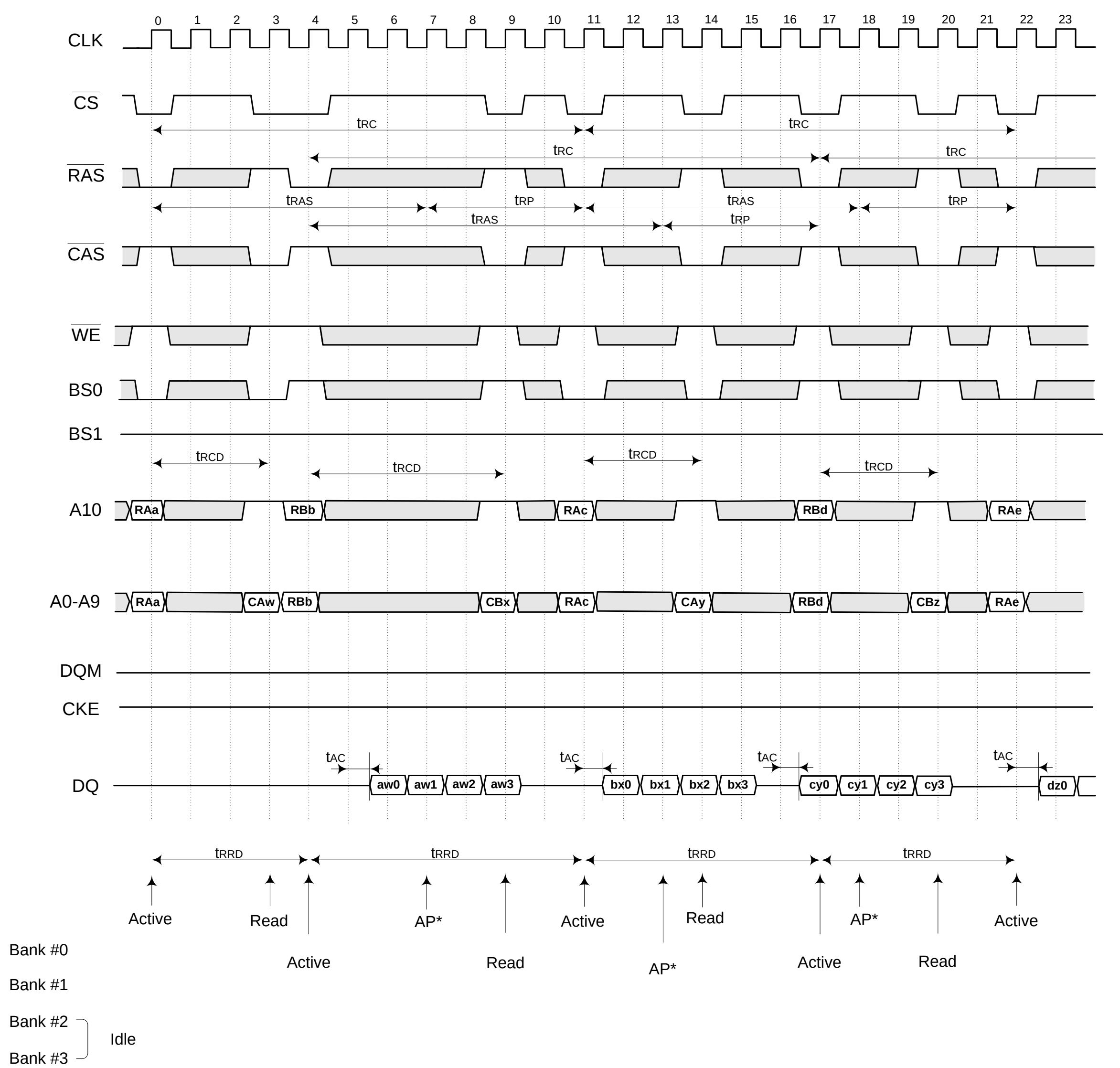
11. OPERATING TIMING EXAMPLE

11.1 Interleaved Bank Read (Burst Length = 4, CAS Latency = 3)



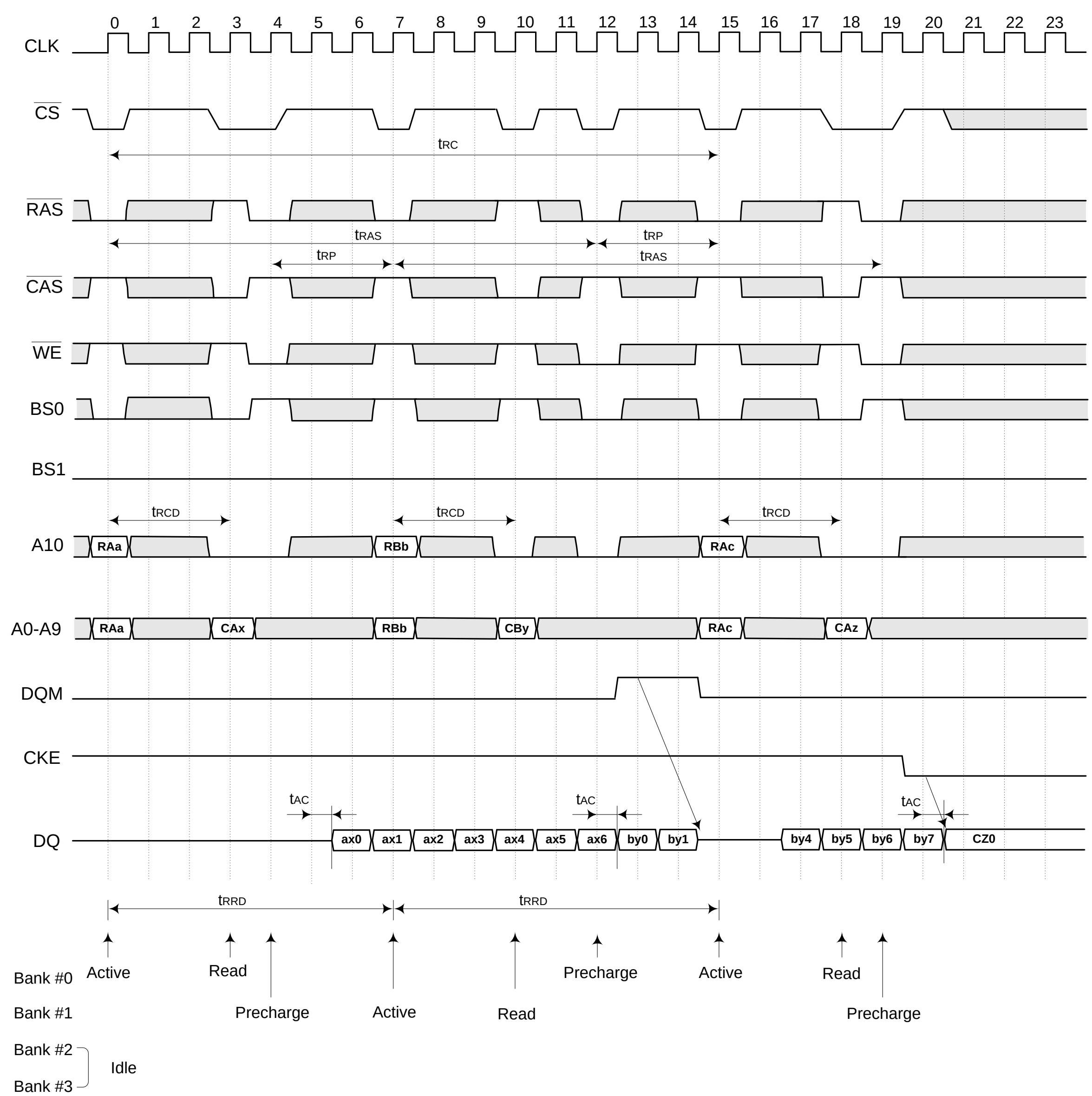
Publication Release Date: Oct. 07, 2013
Revision A02

11.2 Interleaved Bank Read (Burst Length = 4, CAS Latency = 3, Auto-precharge)



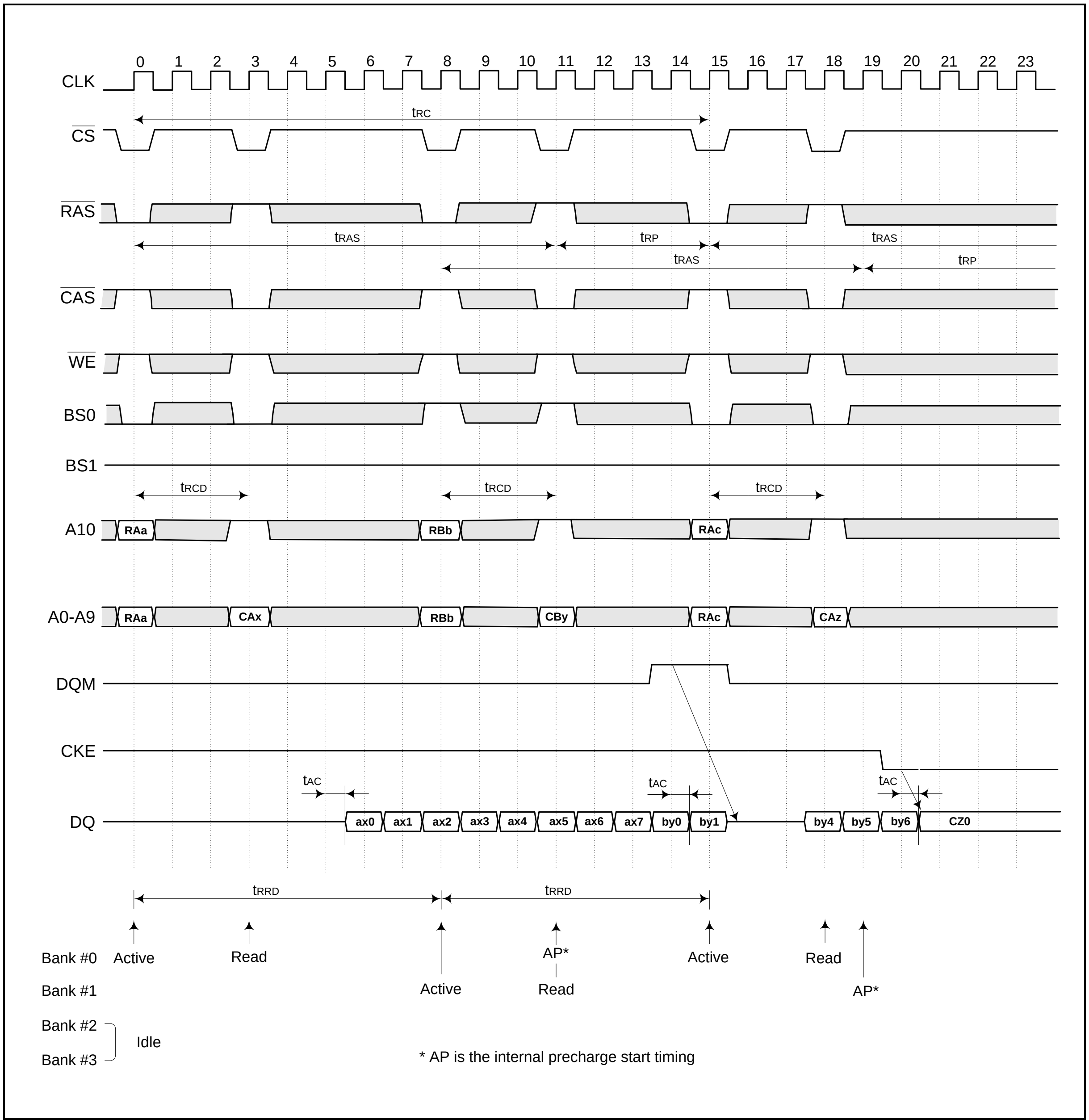
* AP is the internal precharge start timing

11.3 Interleaved Bank Read (Burst Length = 8, CAS Latency = 3)



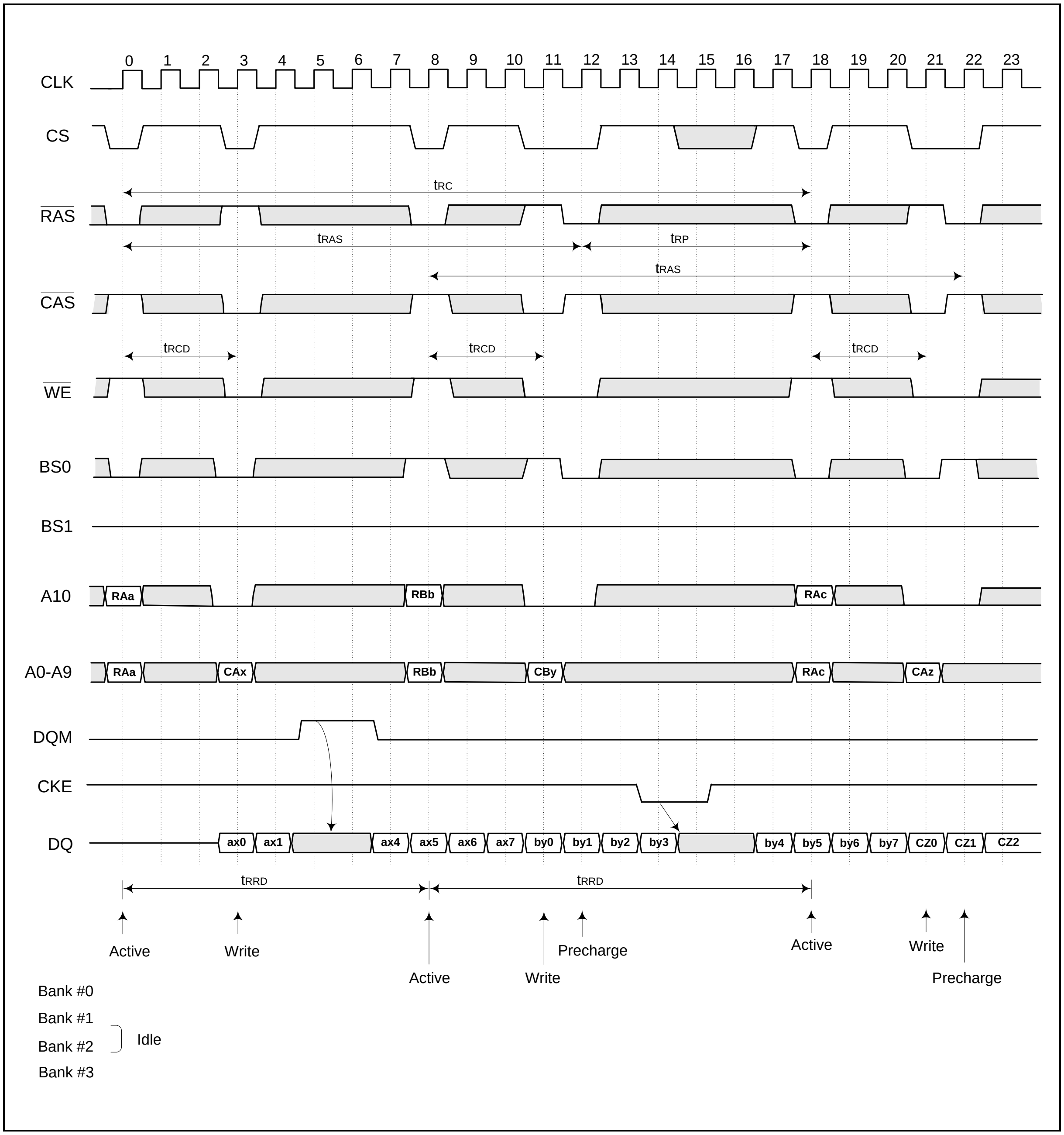
Publication Release Date: Oct. 07, 2013
Revision A02

11.4 Interleaved Bank Read (Burst Length = 8, CAS Latency = 3, Auto-precharge)



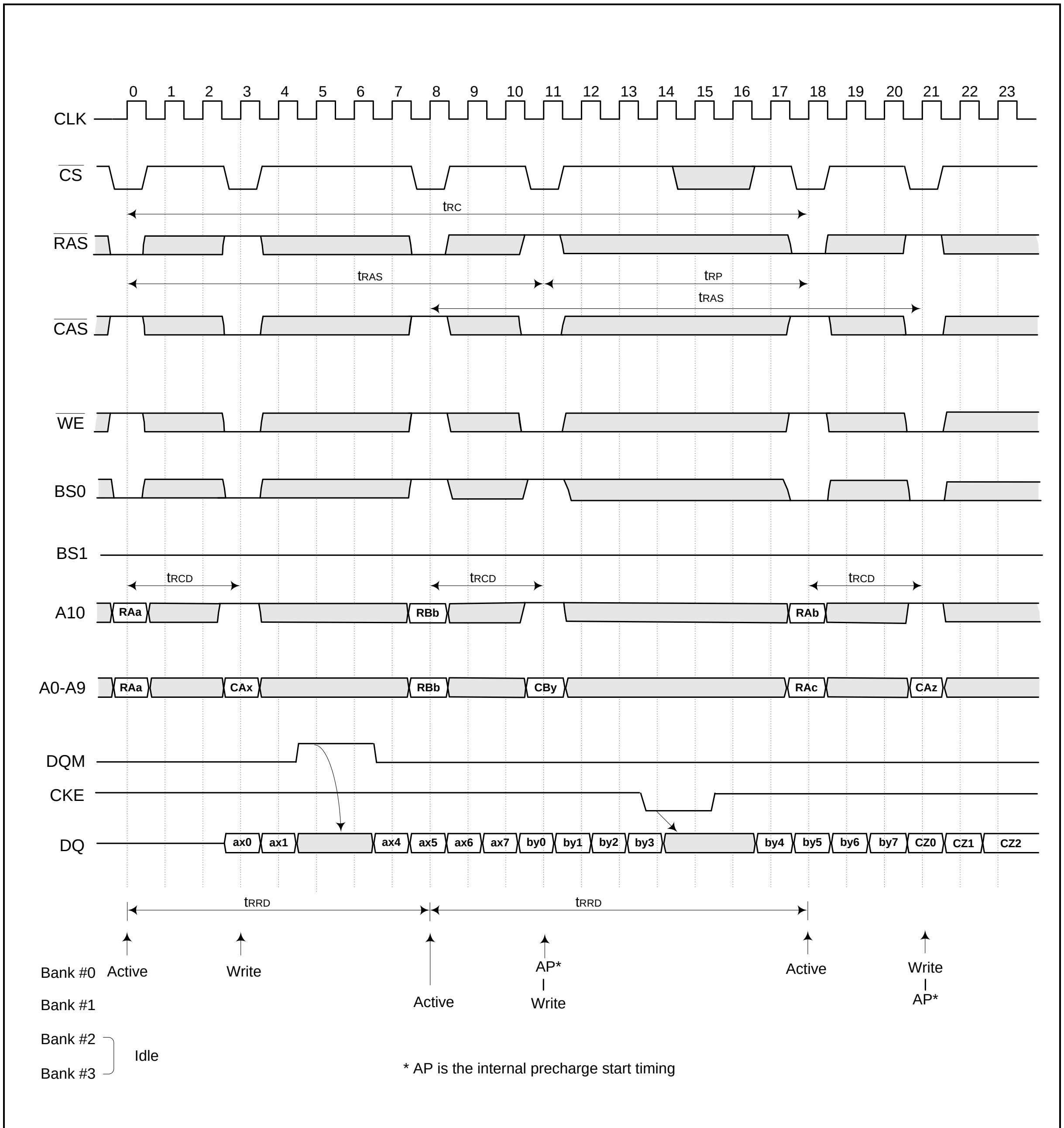
Publication Release Date: Oct. 07, 2013
Revision A02

11.5 Interleaved Bank Write (Burst Length = 8)



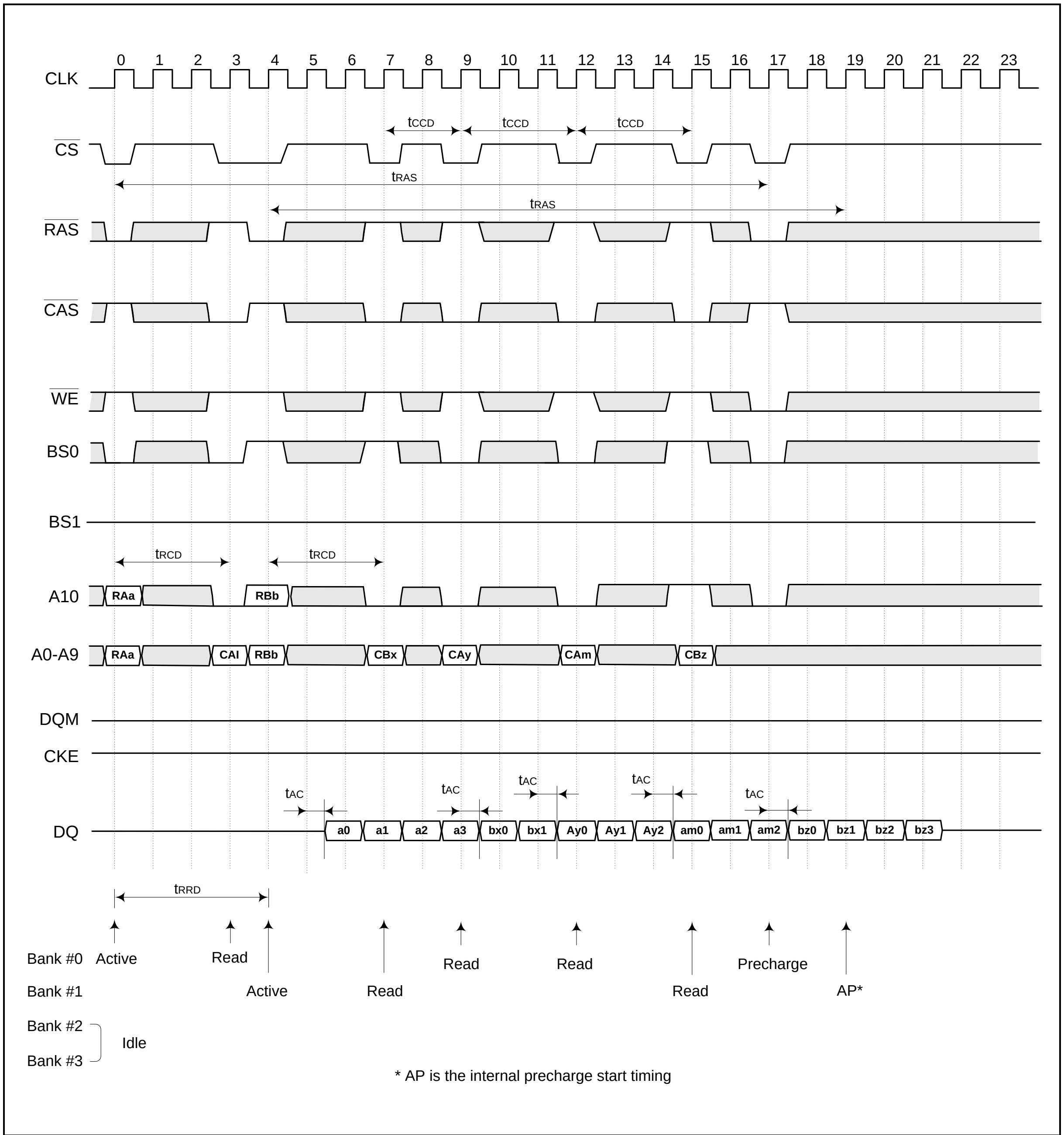
Publication Release Date: Oct. 07, 2013
Revision A02

11.6 Interleaved Bank Write (Burst Length = 8, Auto-precharge)

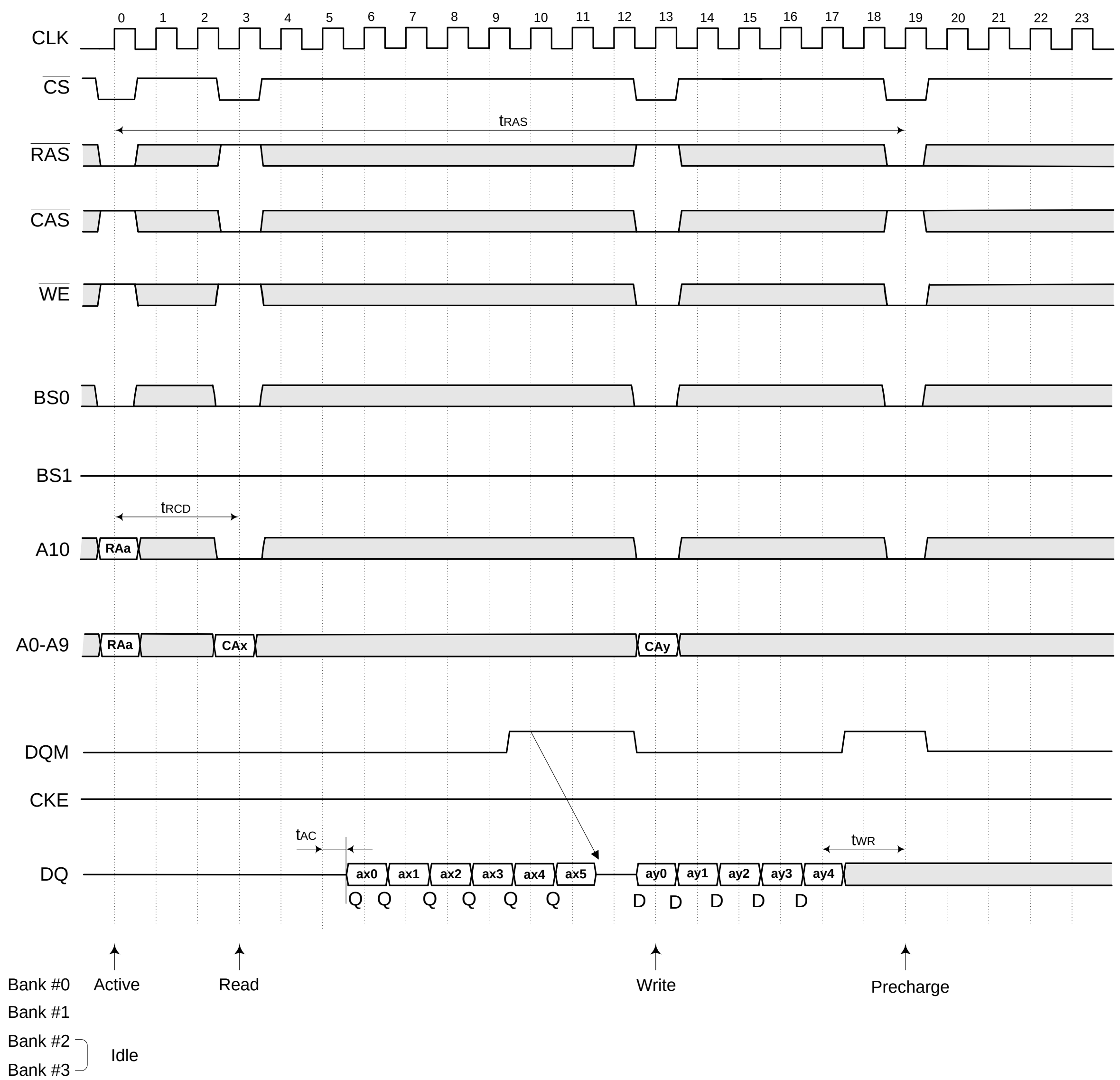


Publication Release Date: Oct. 07, 2013
Revision A02

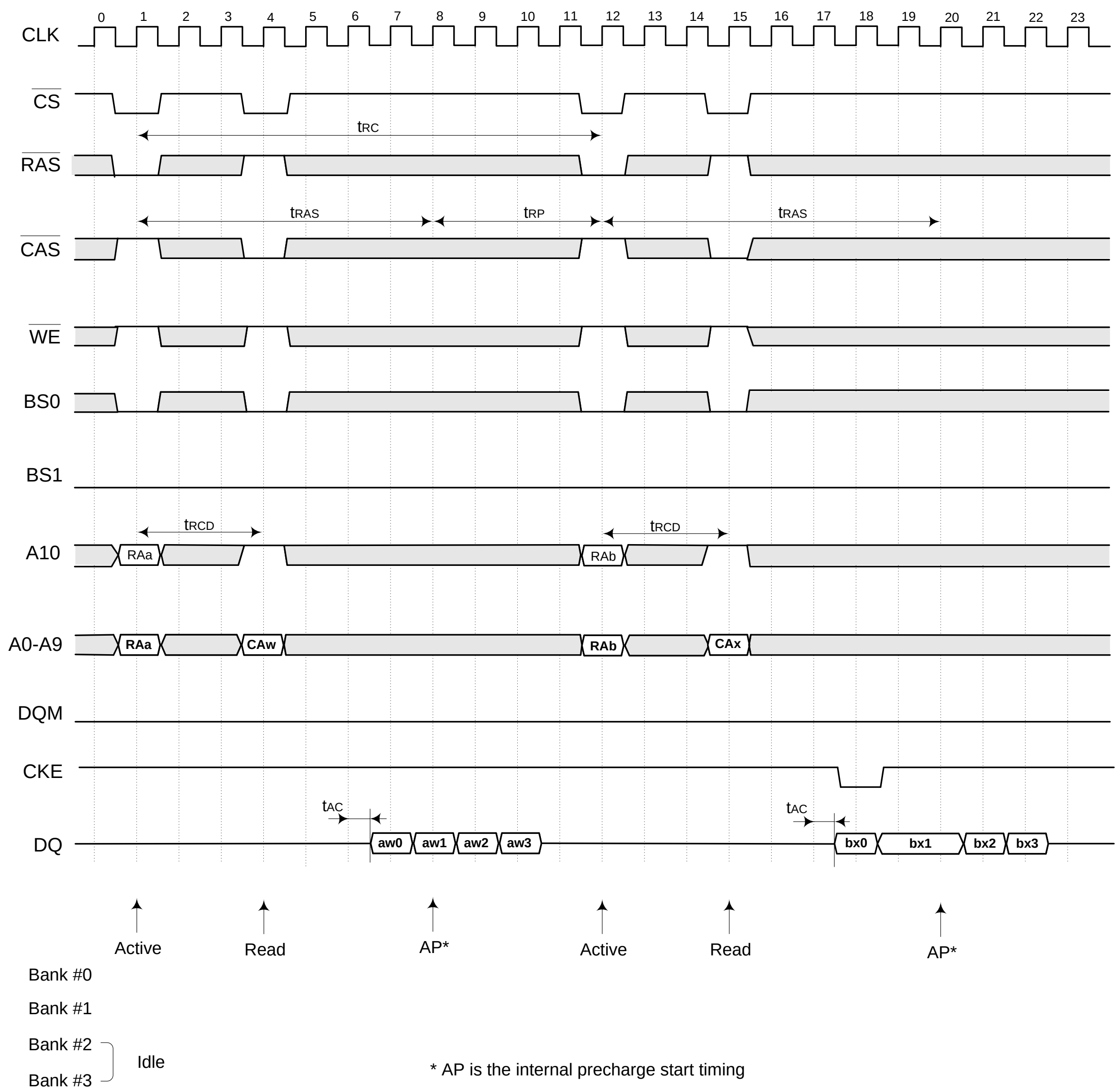
11.7 Page Mode Read (Burst Length = 4, CAS Latency = 3)



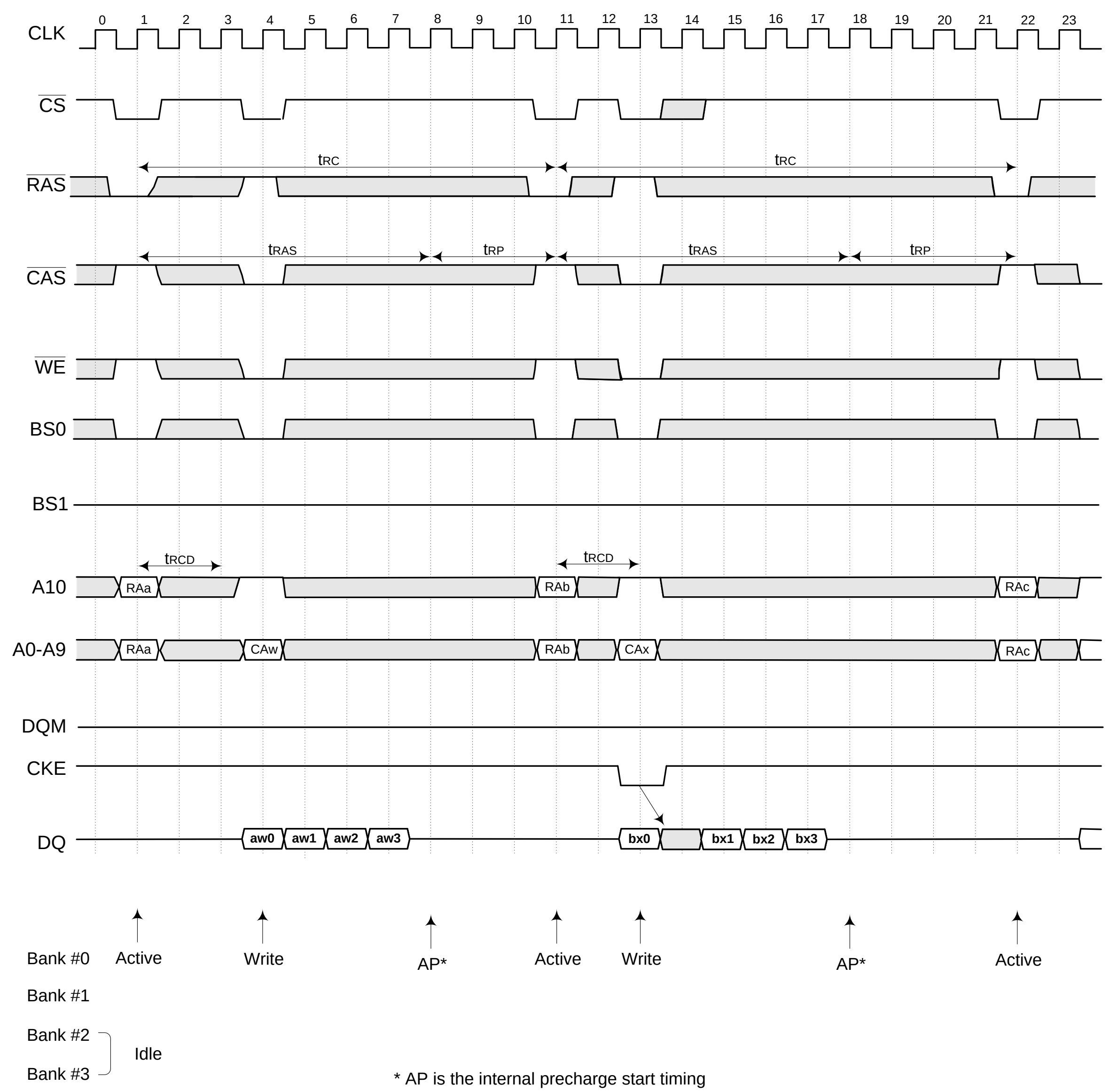
11.8 Page Mode Read/Write (Burst Length = 8, CAS Latency = 3)



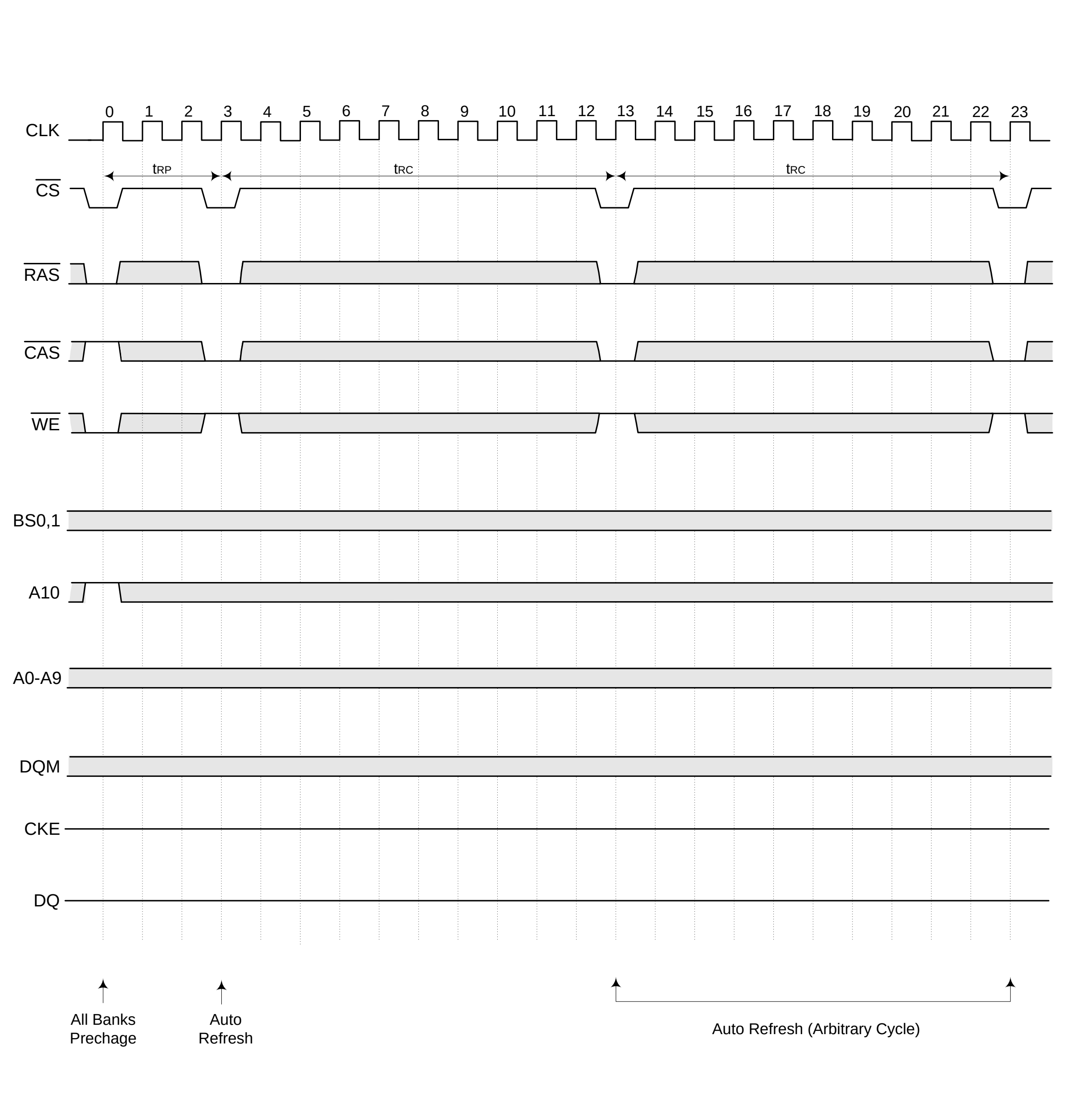
11.9 Auto-precharge Read (Burst Length = 4, CAS Latency = 3)



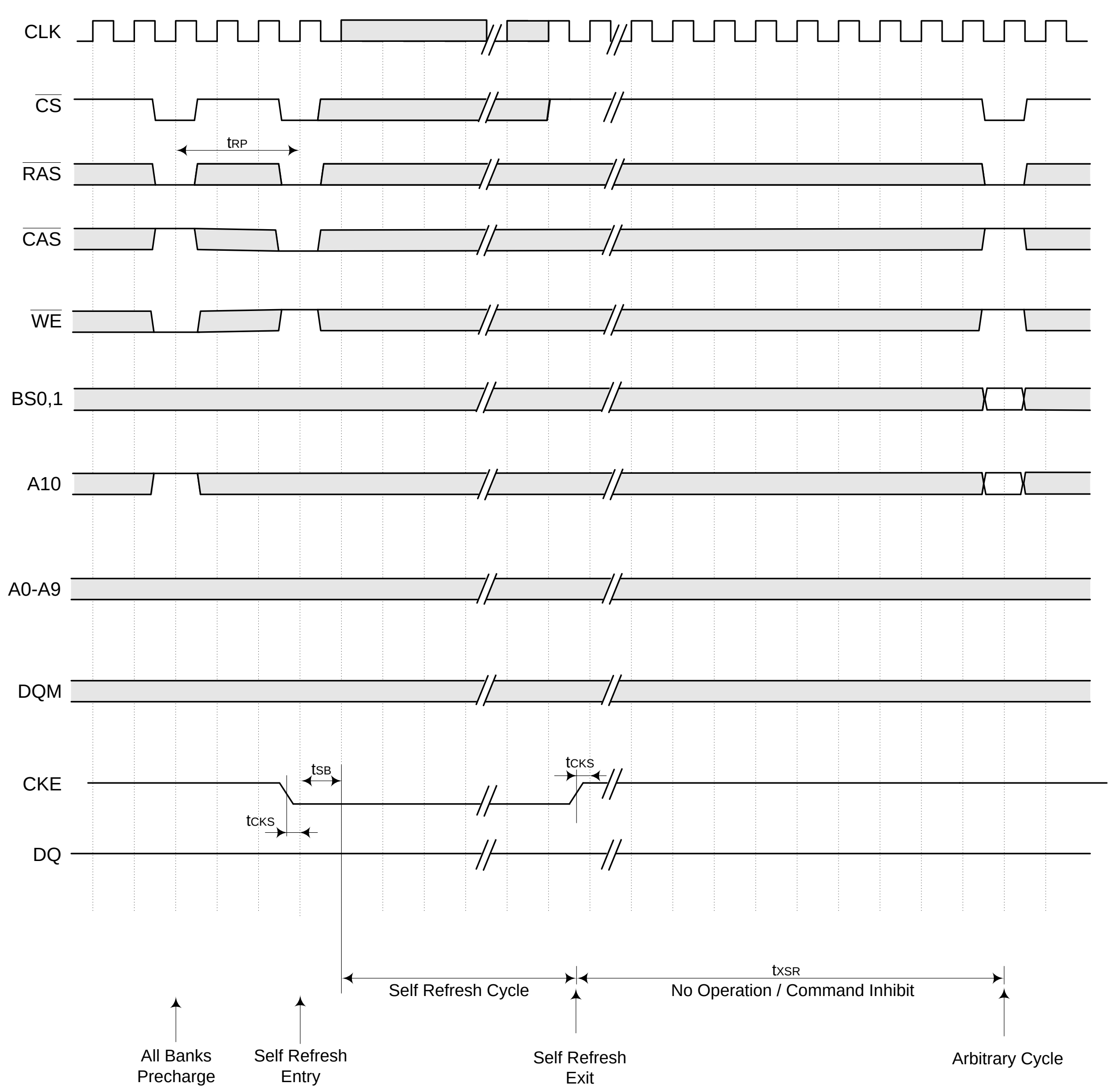
11.10 Auto-precharge Write (Burst Length = 4)



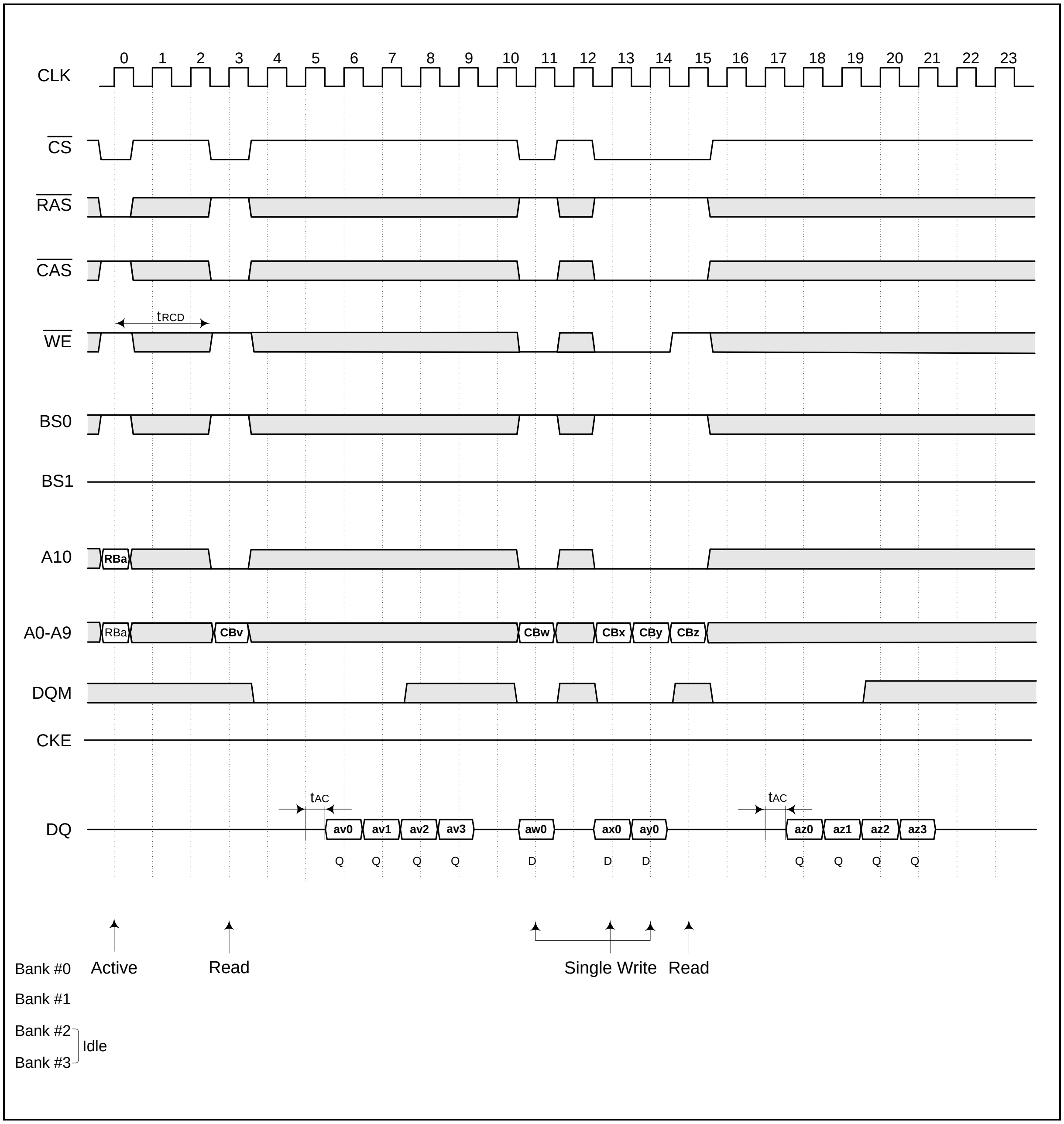
11.11 Auto Refresh Cycle



11.12 Self Refresh Cycle

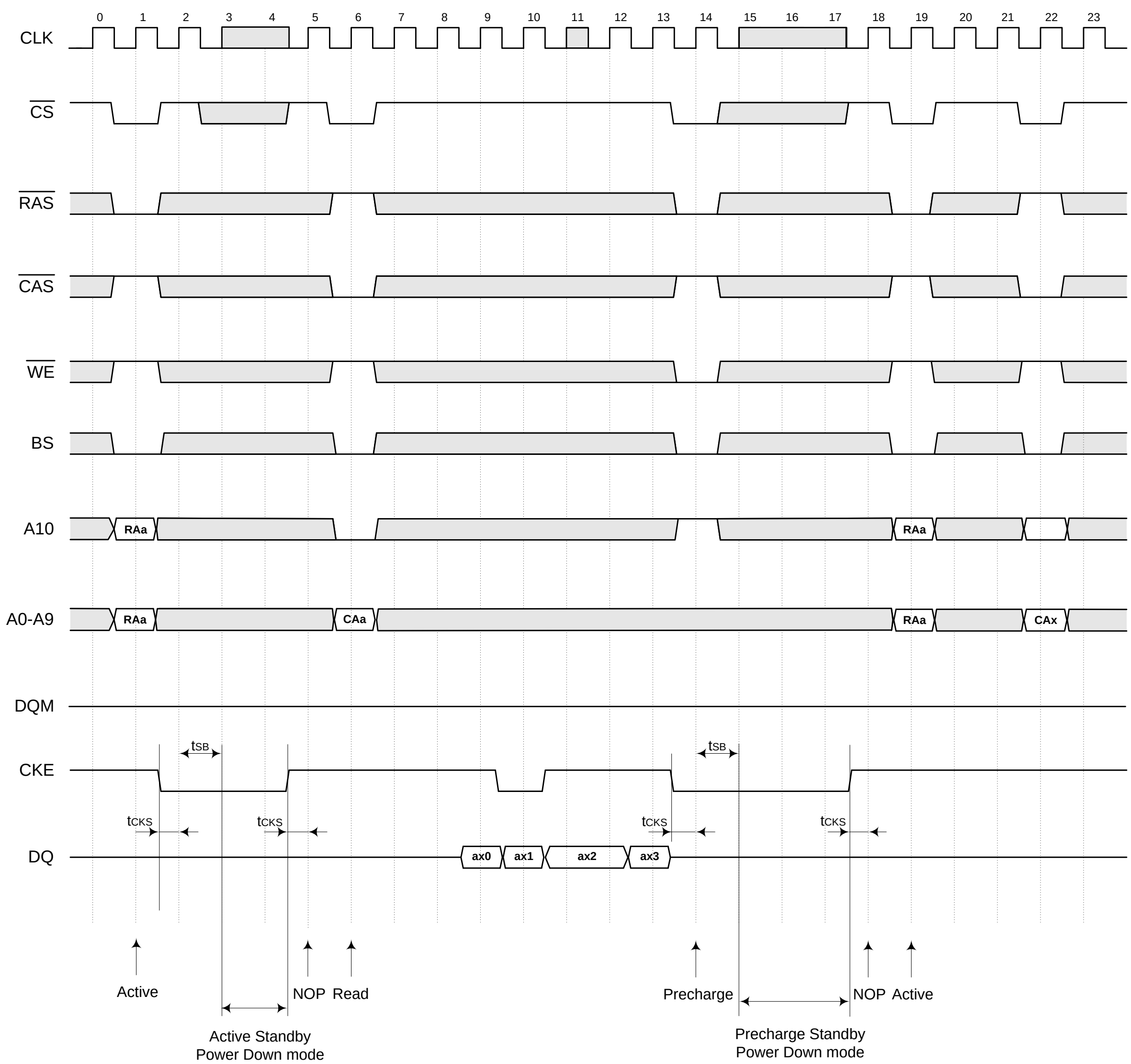


11.13 Bust Read and Single Write (Burst Length = 4, CAS Latency = 3)



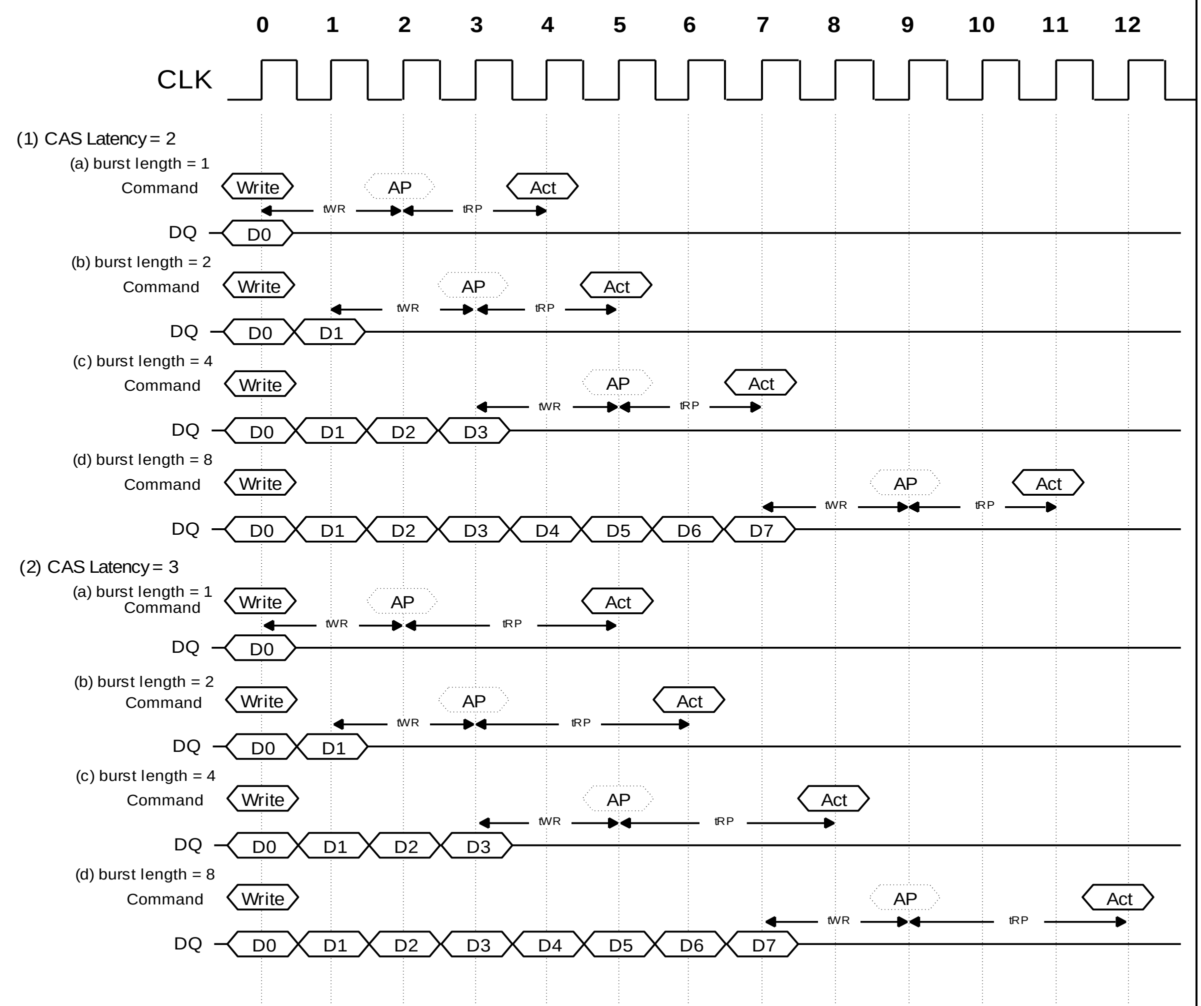
Publication Release Date: Oct. 07, 2013
Revision A02

11.14 Power Down Mode



Note: The Power Down Mode is entered by asserting CKE "low".
All Input/Output buffers (except CKE buffers) are turned off in the Power Down mode.
When CKE goes high, command input must be No operation at next CLK rising edge.
Violating refresh requirements during power-down may result in a loss of data.

11.15 Auto-precharge Timing (Write Cycle)



Note)

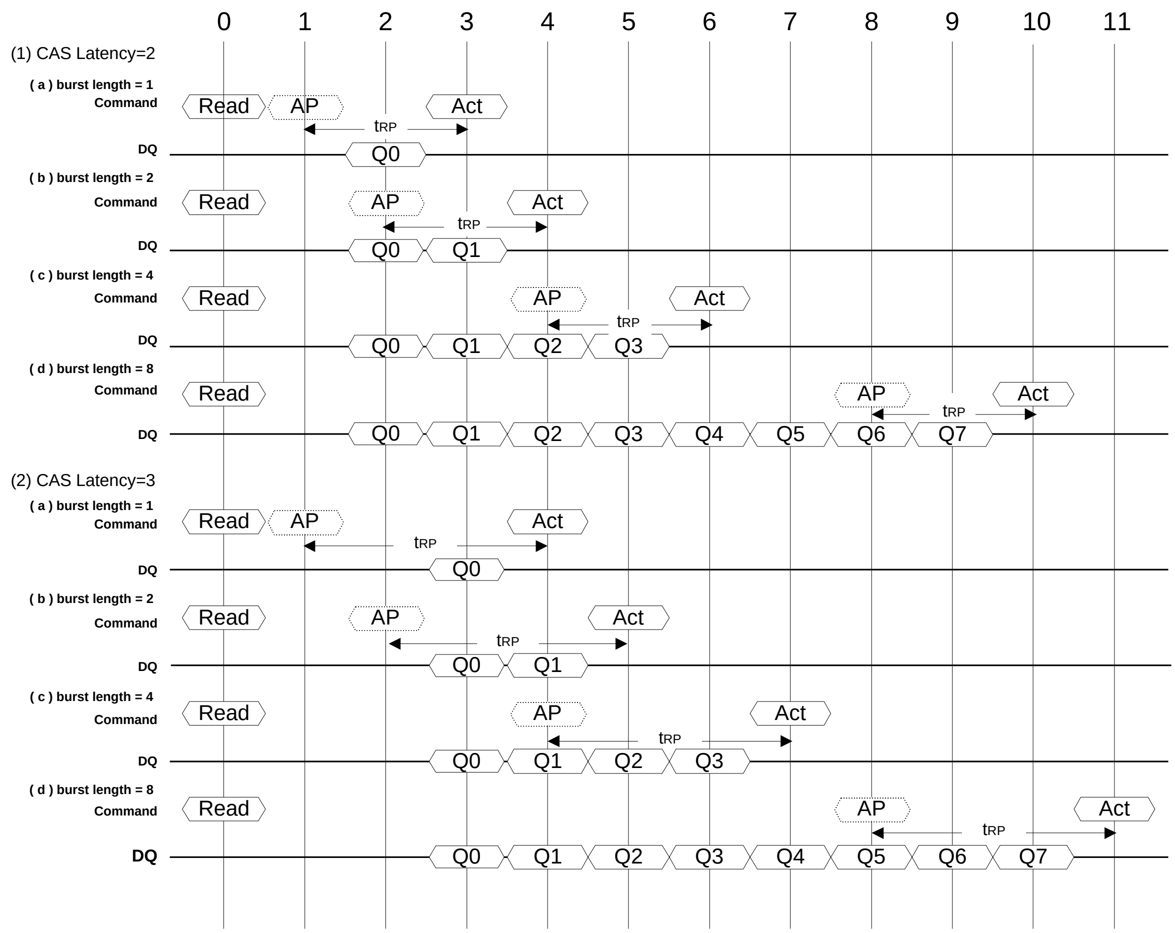
Write represents the Write with Auto precharge command.

AP represents the start of internal precharing.

Act represents the Bank Active command.

When the /auto precharge command is asserted,the period from Bank Activate command to the start of intermal precgarging must be at least tRAS (min).

11.16 Auto-precharge Timing (Read Cycle)



Note:

Read represents the Read with Auto precharge command.

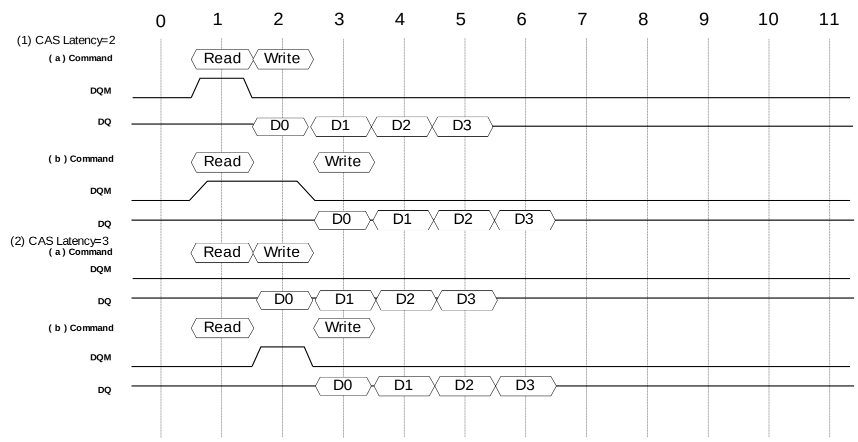
AP represents the start of internal precharging.

Act represents the Bank Activate command.

When the Auto precharge command is asserted, the period from Bank Activate command to the start of internal precgarging must be at least tRAS (min).

11.17 Timing Chart of Read to Write Cycle

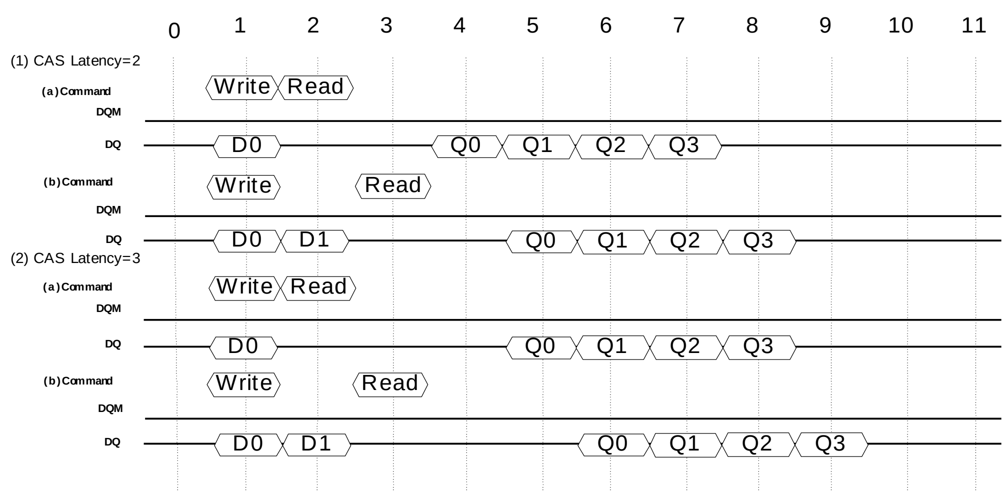
In the case of Burst Length = 4



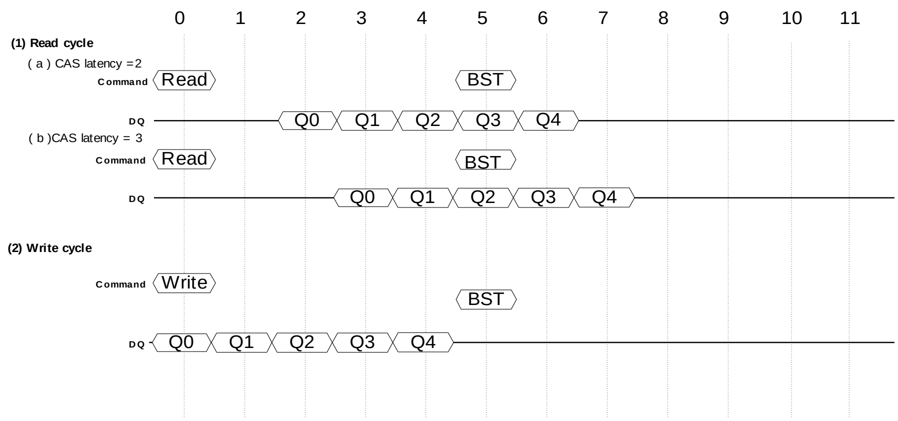
Note: The Output data must be masked by DQM to avoid I/O conflict.

11.18 Timing Chart of Write to Read Cycle

In the case of Burst Length=4

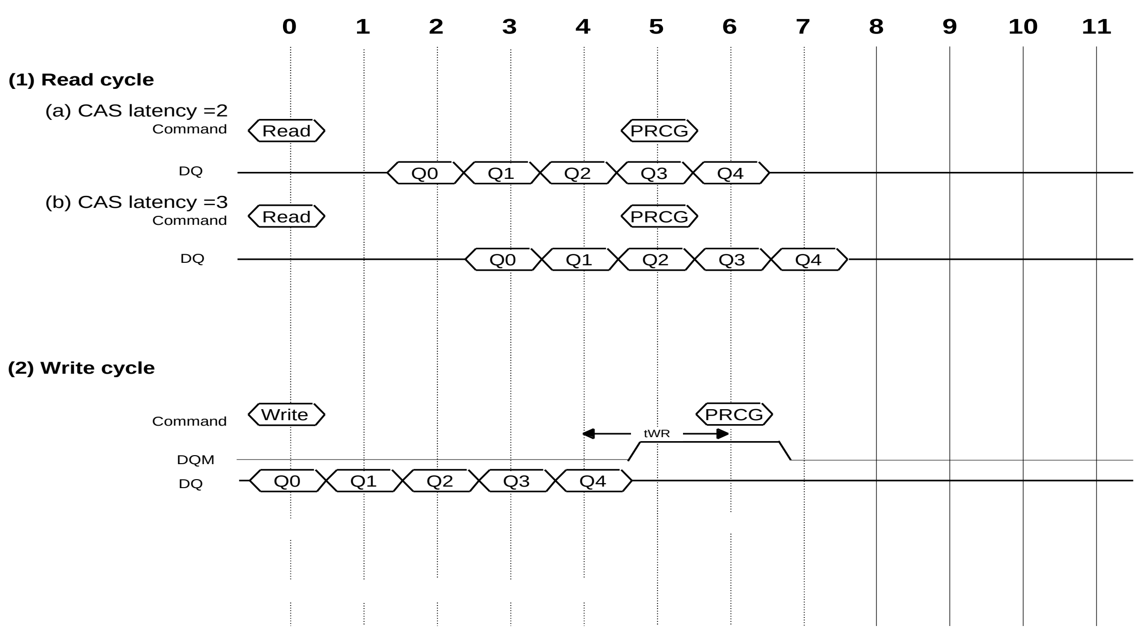


11.19 Timing Chart of Burst Stop Cycle (Burst Stop Command)



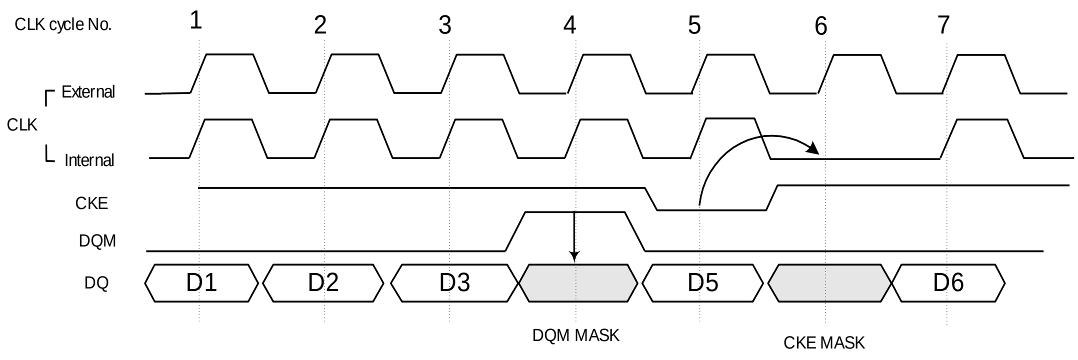
Note: BST represents the Burst stop command

11.20 Timing Chart of Burst Stop Cycle (Precharge Command)

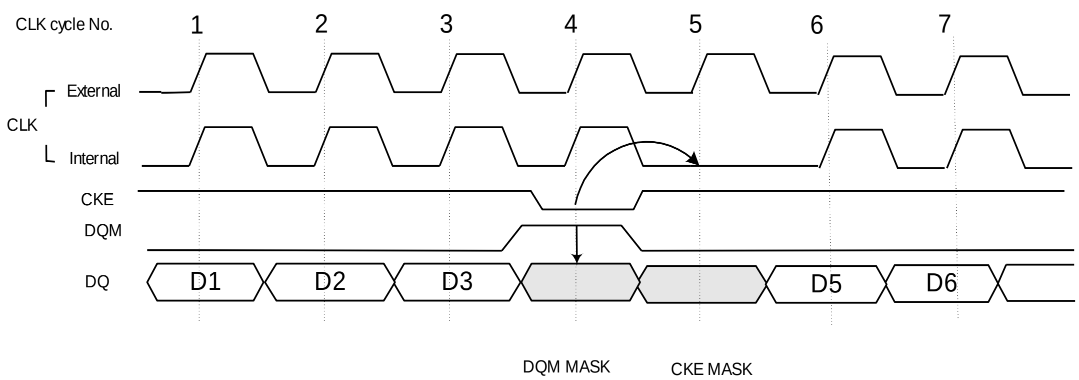


Publication Release Date: Oct. 07, 2013
Revision A02

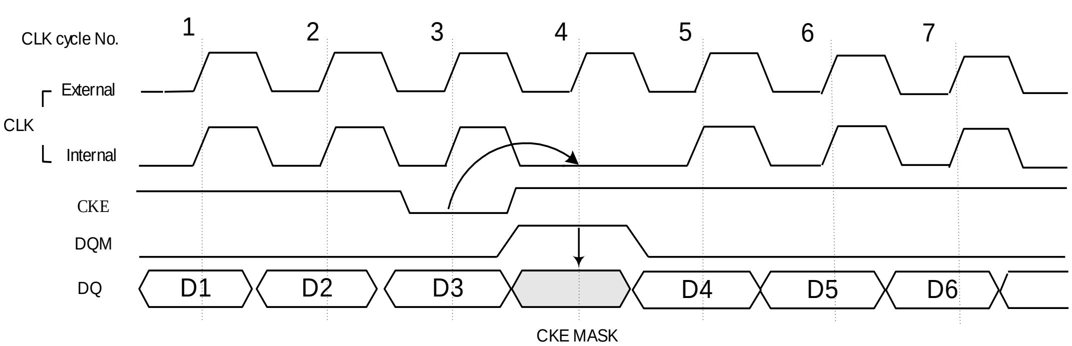
11.21 CKE/DQM Input Timing (Write Cycle)



(1)

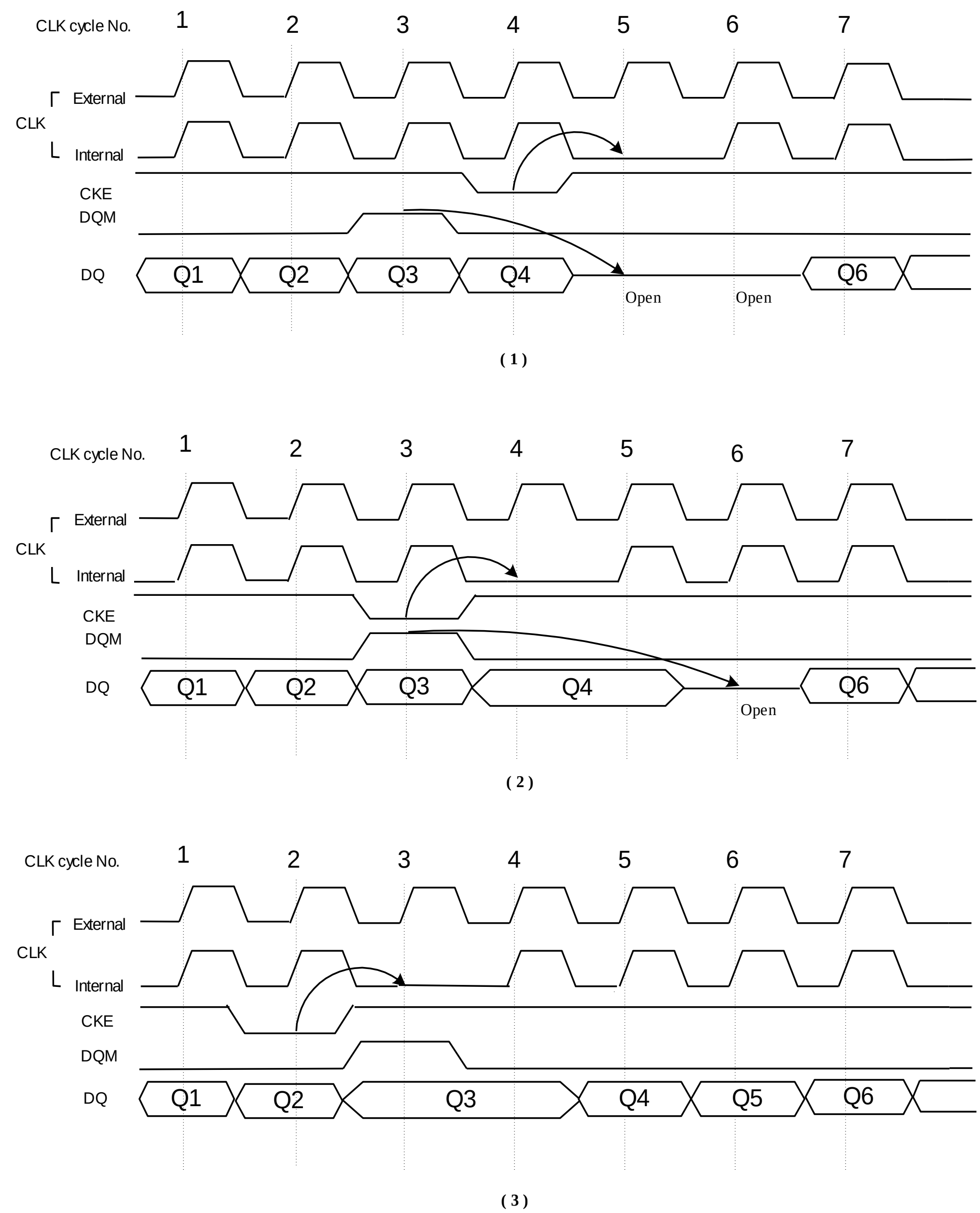


(2)



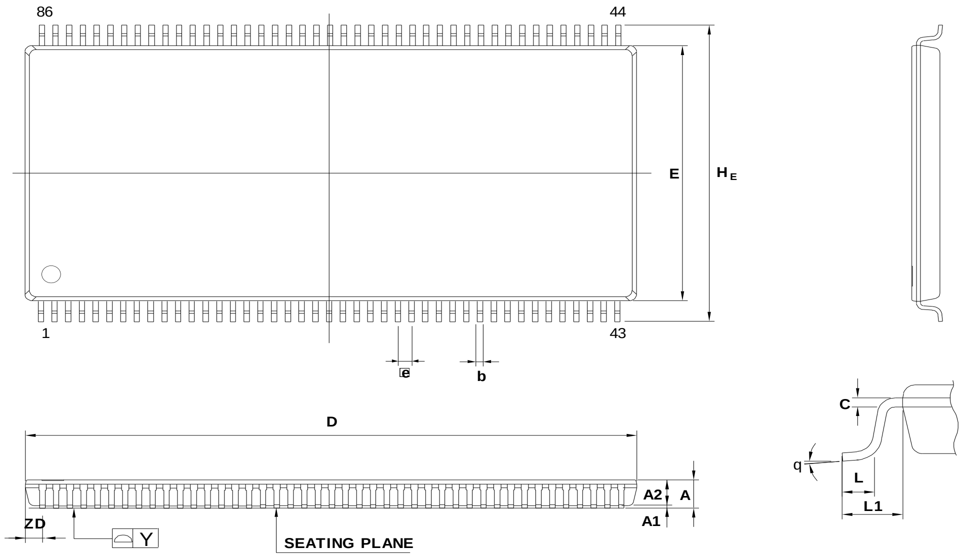
(3)

11.22 CKE/DQM Input Timing (Read Cycle)



12. PACKAGE SPECIFICATION

86L TSOP (II)-400 mil



Controlling Dimension: Millimeters

SYM.	DIMENSION (MM)			DIMENSION (INCH)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.20	—	—	0.047
A1	0.05	—	0.15	0.002	—	0.006
A2	—	1.00	—	—	0.039	—
b	0.17	—	0.27	0.007	—	0.011
c	0.12	—	0.21	0.005	—	0.008
D	22.12	22.22	22.62	0.871	0.875	0.905
E	10.06	10.16	10.26	0.396	0.400	0.404
HE	11.56	11.76	11.96	0.455	0.463	0.471
e	—	0.50	—	—	0.020	—
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	—	0.80	—	—	0.032	—
Y	—	—	0.10	—	—	0.004
ZD	—	0.61	—	—	0.024	—

13. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	Dec. 01, 2011	All	Initial formal datasheet
A02	Oct. 07, 2013	3, 14~16	Added -6K automotive grade parts

Important Notice

Winbond products are not designed, intended, authorized or warranted for use as components in systems or equipment intended for surgical implantation, atomic energy control instruments, airplane or spaceship instruments, transportation instruments, traffic signal instruments, combustion control instruments, or for other applications intended to support or sustain life. Further more, Winbond products are not intended for applications wherein failure of Winbond products could result or lead to a situation wherein personal injury, death or severe property or environmental damage could occur.

Winbond customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Winbond for any damages resulting from such improper use or sales.