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FAIRCHILD SEMICONDUCTOR®

February 2009

SG6901A
CCM PFC/Flyback PWM Combination Controller

Features

- Interleaved PFC/PWM Switching
- Low Startup and Operating Current
- Innovative Switching Charge Multiplier Divider
- Multi-vector Control for Improved PFC Output Transient Response
- Average-Current-Mode Control for PFC
- Programmable Two-Level PFC Output Voltage Protections
- PFC and PWM Feedback Open-Loop Protection
- Cycle-by-Cycle Current Limiting for PFC/PWM
- Slope Compensation for PWM
- H/L Line Over-Power Compensation for PWM
- Brownout Protection
- Over-Temperature Protection (OTP)

Applications

- Switching Power Supplies with Active PFC and Standby Power
- High-Power Adaptors

Description

The highly integrated SG6901A is designed for power supplies with boost PFC and flyback PWM. It requires very few external components to achieve versatile protections. It is available in a 20-pin SOP package.

A proprietary interleave-switching feature synchronizes the PFC and PWM stages and reduces switching noise.

For PFC stage, the proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6901A shuts off PFC to prevent extra-high voltage on output.

For the flyback PWM, the synchronized slope compensation ensures the stability of the current loop under continuous-conduction-mode operation. Built-in line-voltage compensation maintains constant output-power limit. Hiccup operation during output overloading is also guaranteed.

In addition, SG6901A provides protection functions, such as brownout and RI pin open/short protection.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
SG6901ASZ	-30°C to +85°C	RoHS	20-Lead, Small Outline Integrated Circuit (SOIC), JEDEC MS013, .300 inch, Wide Body	Tape & Reel

For Fairchild's definition of "green" Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

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Application Circuit

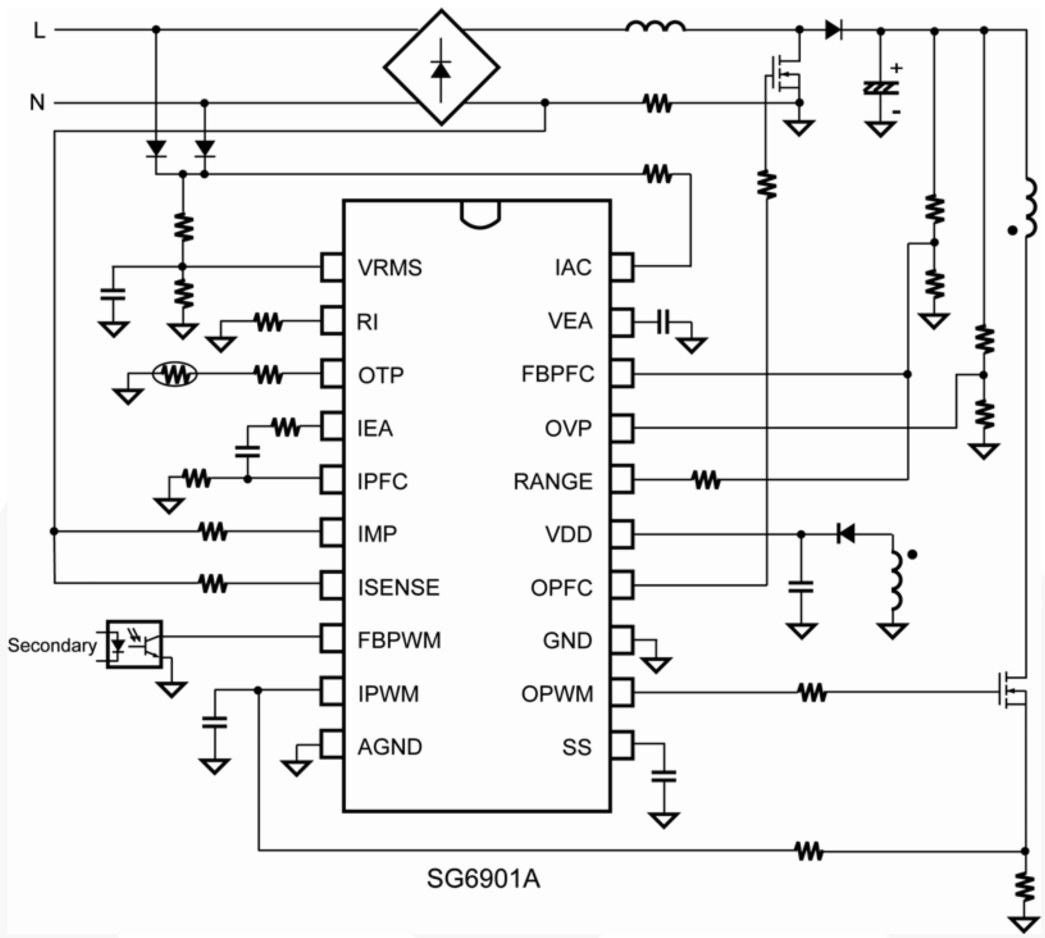

Figure 1. Typical Application

Block Diagram

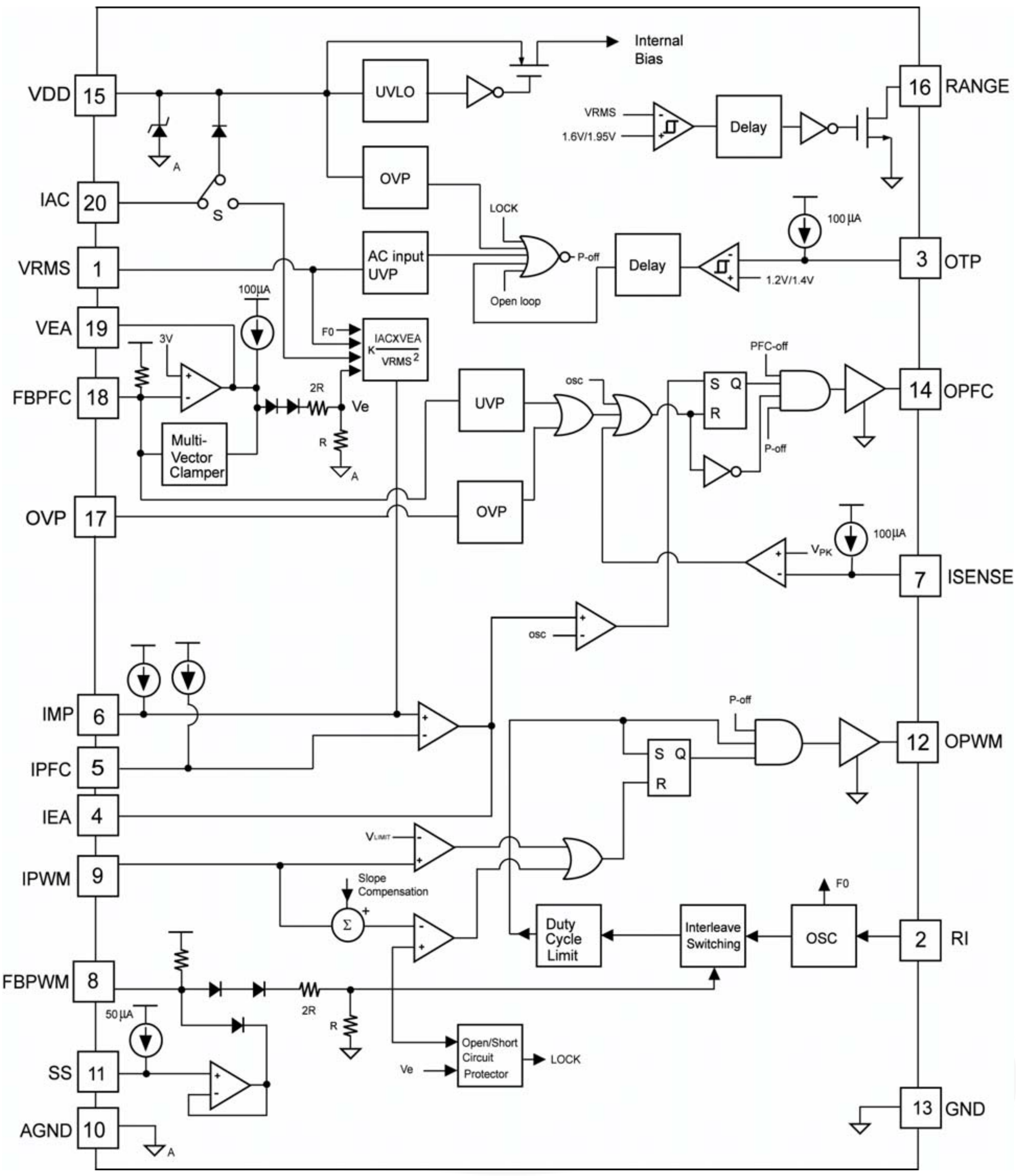

Figure 2. Block Diagram

Marking Information

T- S=SOP
P- Z=Lead Free
Null=regular package
XXXXXXXX- Wafer Lot
Y: Year; WW: Week
V: Assembly Location

Figure 3. Top Mark

Pin Configuration

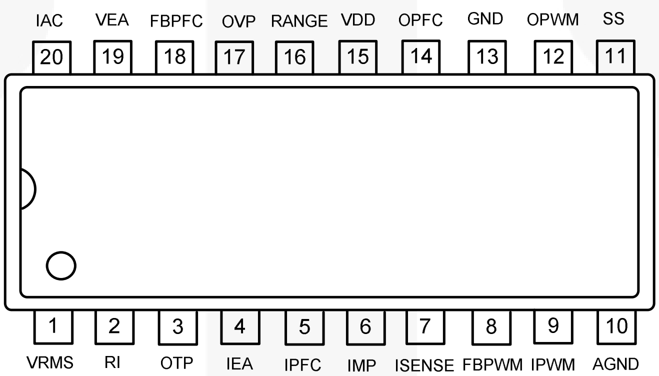

Figure 4. Pin Configuration

Pin Definitions

Pin #	Name	Description
1	VRMS	**Line voltage detection.** The pin is used for PFC multiplier, RANGE control of PFC output voltage, and brownout protection. For brownout protection, the controller is disabled after a delay time when the VRMS voltage drops below a threshold.
2	RI	**Reference setting.** One resistor connected between RI and ground determines the switching frequency. The switching frequency is equal to [1560 / RI] KHz, where R_I is in KΩ. For example, if R_I is equal to 24KΩ, the switching frequency is 65KHz.
3	OTP	**Over-temperature protection.** A constant current is output from this pin. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below the OTP threshold, the SG6901A is disabled.
4	IEA	**PFC current amplifier output.** The signal from this pin is compared with an internal sawtooth to determine the pulse width for PFC gate drive.
5	IPFC	**The inverting input of the PFC current amplifier.** Proper external compensation circuits result in excellent input power factor via average-current-mode control.
6	IMP	**The non-inverting input of the PFC current amplifier and the output of multiplier.** Proper external compensation circuits results in excellent input power factor via average-current-mode control.
7	ISENSE	**Current limit**. A resistor from this pin to GND sets the current limit.
8	FBPWM	**The control input for voltage-loop feedback of PWM stage.** It is internally pulled high through a 6.5kΩ resistance. Usually an external opto-coupler from secondary feedback circuit is connected to this pin.
9	IPWM	**The current-sense input for the flyback PWM.** Via a current sense resistor, this pin provides the control input for peak-current-mode control and cycle-by-cycle current limiting.
10	AGND	Signal ground.
11	SS	**Soft start.** During startup, the SS pin charges an external capacitor with a 50μA (R_I=24KΩ) constant current source. The voltage on FBPWM is clamped by SS during startup. In the event of a protection condition occurring and/or PWM being disabled, the SS pin is quickly discharged.
12	OPWM	The totem-pole output drive for the flyback PWM MOSFET. This pin is internally clamped under 17V to protect the MOSFET.
13	GND	Power ground.
14	OPFC	**The totem-pole output drive for the PFC MOSFET.** This pin is internally clamped under 17V to protect the MOSFET.
15	VDD	The power supply pin.
16	RANGE	**The RANGE pin has high impedance** whenever the V_{RMS} voltage is lower than a threshold. The PFC output voltage at low line can be reduced to improve efficiency.
17	OVP	**The PFC stage over-voltage input.** The comparator disables the PFC output driver if the voltage at this input exceeds a threshold. This pin can be connected to FBPFC or it can be connected to the PFC boost output through a divider network.
18	FBPFC	**The feedback input for PFC voltage loop.** The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
19	VEA	**The error amplifier output for PFC voltage feedback loop.** A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
20	IAC	**This input** is used to provide current reference for the multiplier.

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Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{DD}	DC Supply Voltage			25	V
I_{AC}	Input AC Current			2	mA
V_{HIGH}	OPWM, OPFC, IAC		-0.3	25.0	V
V_{LOW}	Others		-0.3	7.0	V
P_D	Power Dissipation at T_A< 50℃			1.15	W
T_J	Operating Junction Temperature		-40	+125	°C
T_{STG}	Storage Temperature Range		-55	+150	°C
Θ_{JC}	Thermal Resistance (Junction-to-Case)			+23.64	°C/W
T_L	Lead Temperature (Soldering)			+260	°C
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		4.5	KV
		Machine Model, JESD22-A115		250	V

Notes:
1. All voltage values, except differential voltage, are given with respect to GND pin.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Operating Ambient Temperature	-30	+85	°C

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VDD SECTION						
V_{DD-OP}	Continuously Operating Voltage				20	V
I_{DD-ST}	Startup Current	0V < V_{DD} < V_{DD-ON}		10	25	µA
I_{DD-OP}	Operating Current	V_{DD}=15V; OPFC, OPWM Open; R_I=24KΩ		6	10	mA
V_{DD-ON}	Start Threshold Voltage		11	12	13	V
V_{DD-OFF}	Minimum Operating Voltage		9	10	11	V
V_{DD-OVP}	V_{DD} OVP Threshold		23.5	24.5	25.5	V
$t_{D-VDDOVP}$	Debounce Time of V_{DD} OVP		8		25	µs
OSCILLATOR SECTION						
f_{OSC}	PWM Frequency	R_I=24KΩ	62	65	68	KHz
R_I	RI Pin Resistance Range		15.6		47.0	KΩ
R_{I-OPEN}	RI Pin Open Protection	If R_I>R_{I-OPEN}, SG6901A Turns Off		200		KΩ
$R_{I-SHORT}$	RI Pin Short Protection	If R_I<$R_{I-SHORT}$, SG6901A Turns Off		2		KΩ
VRMS SECTION (for UVP and RANGE)						
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Protection Threshold (with t_{UVP} delay)		0.75	0.80	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on V_{RMS}		$V_{RMS-UVP-1}$ + 0.16V	$V_{RMS-UVP-1}$ + 0.18V	$V_{RMS-UVP-1}$ + 0.2V	V
t_{D-PWM}	When UVP Occurs, Interval from PFC Off to PWM Off		$t_{UVP-Min}$+9		$t_{UVP-Min}$+14	ms
t_{UVP}	Under-Voltage Protection Delay Time		150	195	240	ms
V_{RMS-H}	High V_{RMS} Threshold for RANGE Comparator		1.90	1.95	2.00	V
V_{RMS-L}	Low V_{RMS} Threshold for RANGE Comparator		1.55	1.60	1.65	V
t_{RANGE}	Range-Enable Delay Time		140	170	200	ms
V_{OL}	Output Low Voltage of RANGE Pin	I_o=1mA			0.5	V
I_{OH}	Output High Leakage Current of RANGE Pin	RANGE=5V			50	nA

Continued on the following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PFC STAGE						
Voltage Error Amplifier						
V_{REF}	Reference Voltage		2.95	3.00	3.05	V
Av	Open-Loop Gain			60		dB
Z_o	Output Impedance			110		KΩ
OVP_{PFC}	PFC Over-Voltage Protection (OVP Pin)		3.20	3.25	3.30	V
$\triangle OVP_{PFC}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$t_{OVP-PFC}$	Debounce Time of PFC OVP		40	70	120	μs
$V_{FBPFC-H}$	Clamp-High Feedback Voltage		3.10	3.15	3.20	V
$G_{FBPFC-H}$	Clamp-High Gain			0.5		μA/mV
$V_{FBPFC-L}$	Clamp-Low Feedback Voltage		2.75	2.85	2.90	V
$G_{FBPFC-L}$	Clamp-Low Gain			6.5		mA/mV
$I_{FBPFC-L}$	Maximum Source Current		1.5	2.0		mA
$I_{FBPFC-H}$	Maximum Sink Current		70	110		μA
UVP_{FBPFC}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
$t_{UVP-FBPFC}$	Debounce Time of PFC UVP		40	70	120	μs
CURRENT ERROR AMPLIFIER						
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-Loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common Mode Rejection Ratio	V_{CM}=0 to +1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current Source	R_I=24KΩ (I_{MR}=20+I_{RI}•0.8)	50		70	μA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current			0.25		mA

Continued on the following page…

Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PEAK CURRENT LIMIT						
I_P	Constant Current Output	R_I=24KΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{SENSE} < V_{PK})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading-Edge Blanking Time		270	350	450	ns
MULTIPLIER						
I_{AC}	Input AC Current	Multiplier Linear Range	0		360	μA
I_{MO-max}	Maximum Multiplier Current Output	R_I=24KΩ		250		μA
I_{MO-1}	Multiplier Current Output (Low-line, High-Power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=7.5V; R_I=24KΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (High-line, High-Power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=7.5V; R_I=24KΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V
PFC OUTPUT DRIVER						
V_Z	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PFC}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
t_{PFC}	Interval OPFC Lags Behind OPWM at Startup		9.0	11.5	14.0	ms
V_{OH-PFC}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PFC}	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	40	70	120	ns
t_{F-PFC}	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	40	60	110	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%
PWM STAGE						
FBPWM						
A_{v-PWM}	FB to Current Comparator Attenuation		2.5	3.1	3.5	V/V
Z_{FB}	Input Impedance		4	5	7	KΩ
I_{FB}	Maximum Source Current		0.8	1.2	1.5	mA
$FB_{OPEN-LOOP}$	PWM Open-Loop Protection Voltage		4.2	4.5	4.8	V
$t_{OPEN-PWM}$	PWM Open-Loop Protection Delay Time		45	56	70	ms
$t_{OPEN-PWM-Hiccup}$	Interval of PWM Open-Loop Protection Reset		450	600	750	ms

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Electrical Characteristics

V_{DD}=15V and T_A=25°C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
PWM CURRENT SENSE						
t_{PD-PWM}	Propagation Delay to Output	V_{DD}=15V, OPWM<=9V	60		120	ns
$V_{LIMIT-1}$	Peak Current Limit Threshold Voltage1	RANGE=Open	0.65	0.70	0.75	V
$V_{LIMIT-2}$	Peak Current Limit Threshold Voltage2	RANGE=Ground	0.60	0.65	0.70	V
$t_{LEB-PWM}$	Leading-Edge Blanking Time		270	350	450	ns
$\triangle V_{SLOPE}$	Slope Compensation	$\triangle V_S = \triangle V_{SLOPE}$ x (T_{on}/T) $\triangle V_S$: Compensation Voltage Added to Current Sense	0.45	0.50	0.55	V
PWM OUTOUT DRIVER						
V_{Z-PWM}	Output Voltage Maximum (Clamp)	V_{DD}=20V		16	18	V
V_{OL-PWM}	Output Voltage Low	V_{DD}=15V; I_O=100mA			1.5	V
V_{OH-PWM}	Output Voltage High	V_{DD}=13V; I_O=100mA	8			V
t_{R-PWM}	Rising Time	V_{DD}=15V; C_L=5nF; O/P=2V to 9V	30	60	120	ns
t_{F-PWM}	Falling Time	V_{DD}=15V; C_L=5nF; O/P=9V to 2V	30	50	110	ns
DCY_{MAXPWM}	Maximum Duty Cycle		73	78	83	%
OTP SECTION						
I_{OTP}	OTP Pin Output Current	R_I=24KΩ	90	100	110	μA
V_{OTP-ON}	Recovery Level on OTP		1.35	1.40	1.45	V
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
t_{OTP}	OTP Debounce Time		8		25	μs
SOFT START SECTION						
I_{SS}	Constant Current Output for Soft-Start	R_T=24KΩ	44	50	56	μA
R_D	Discharge R_{DSON}			470		Ω

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Typical Performance Characteristics

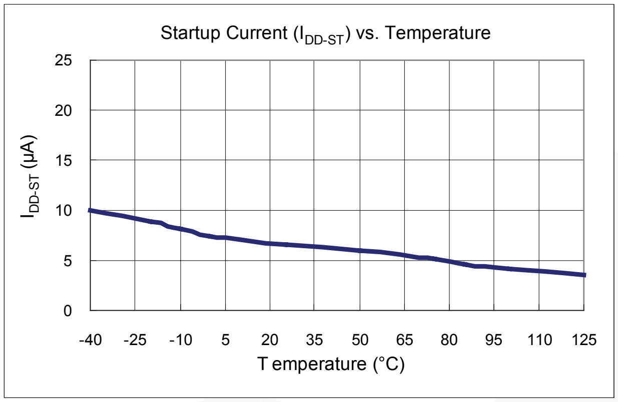

Figure 5. Startup Current

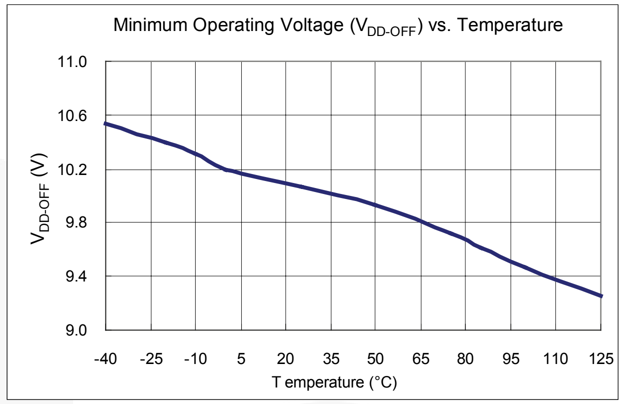

Figure 6. V_{DD} Turn-Off Threshold Voltage

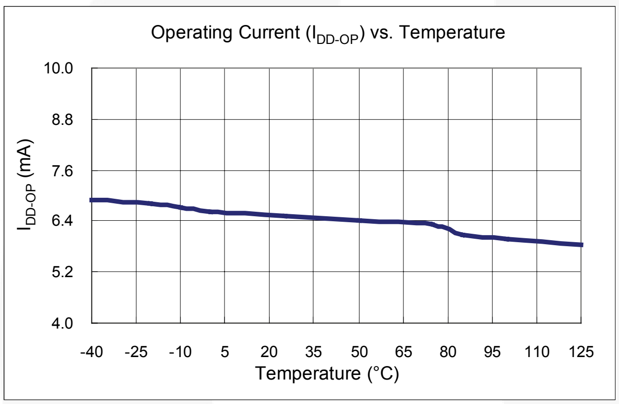

Figure 7. Operating Current

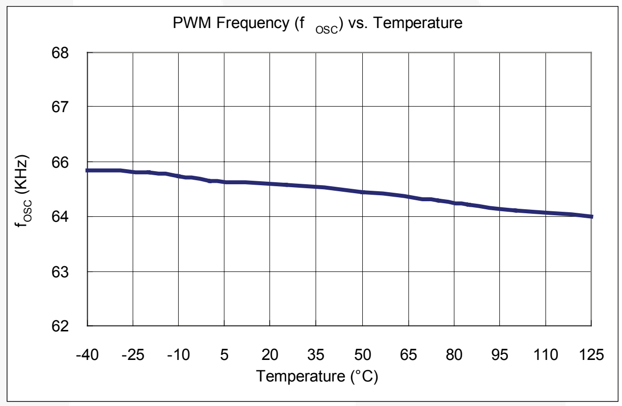

Figure 8. PWM Frequency

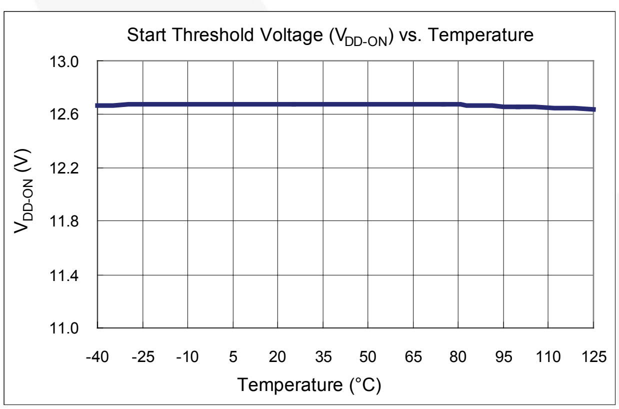

Figure 9. V_{DD} Turn-On Threshold Voltage

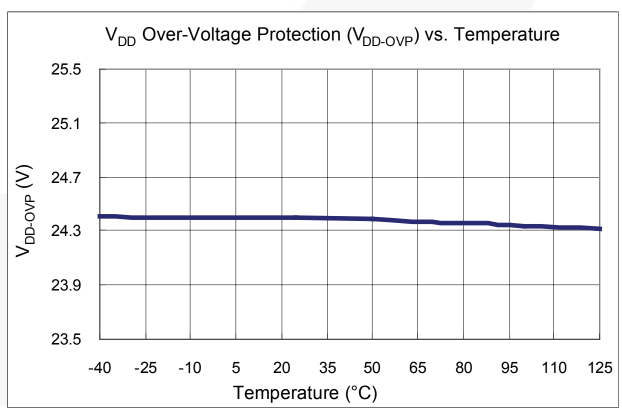

Figure 10. V_{DD} OVP Threshold Voltage

Typical Performance Characteristics

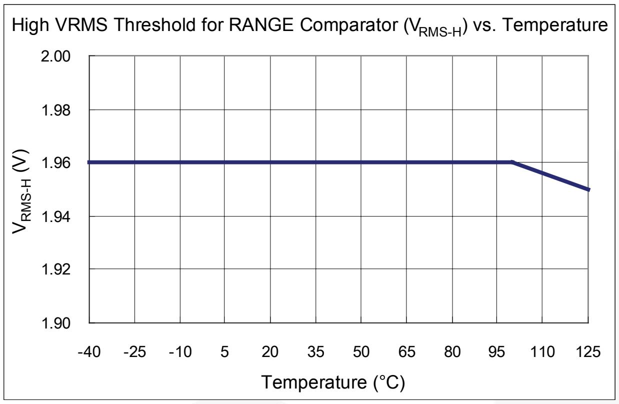

Figure 11. High V_{RMS} Threshold for RANGE Comparator

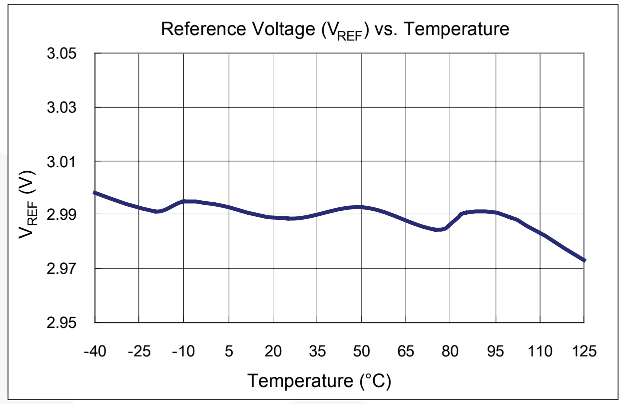

Figure 12. Reference Voltage

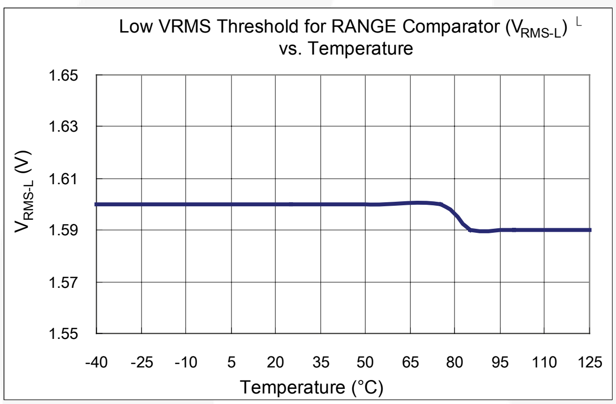

Figure 13. Low V_{RMS} Threshold for RANGE Comparator

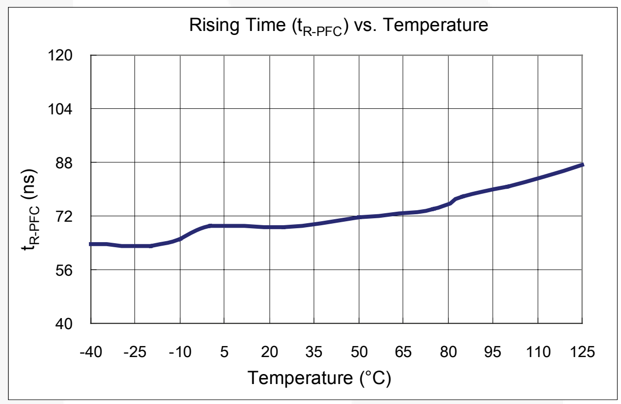

Figure 14. OPFC Rising Time

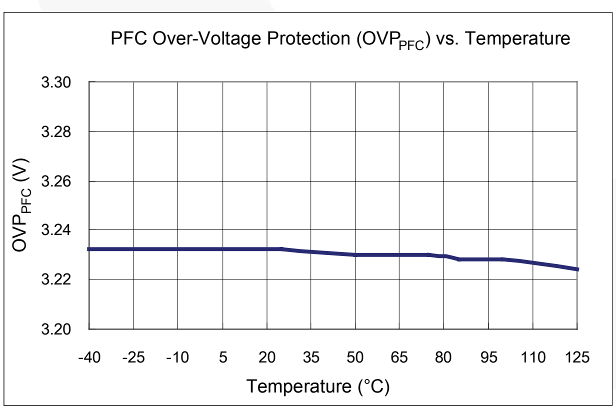

Figure 15. PFC OVP Threshold Voltage

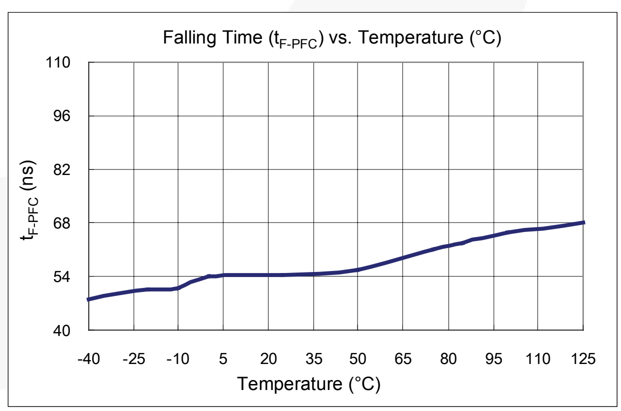

Figure 16. OPFC Falling Time

Typical Performance Characteristics

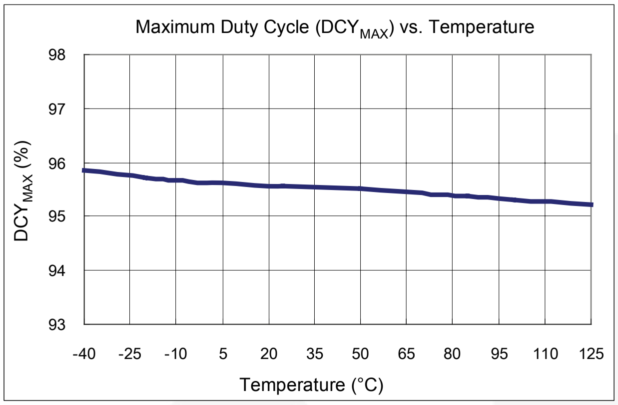

Figure 17. PFC Maximum Duty Cycle

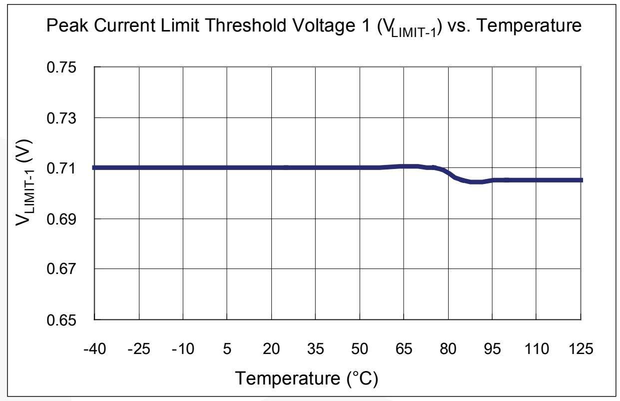

Figure 18. Peak Current Limit Threshold Voltage

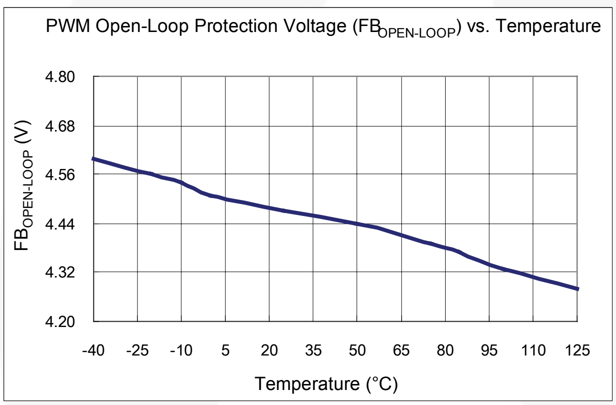

Figure 19. PWM Open-Loop Protection Voltage

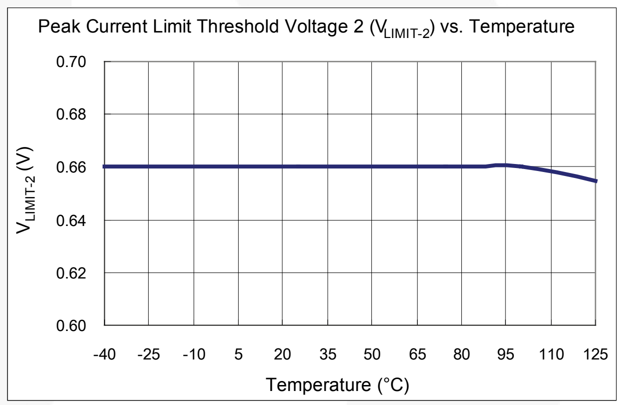

Figure 20. Peak Current Limit Threshold Voltage2

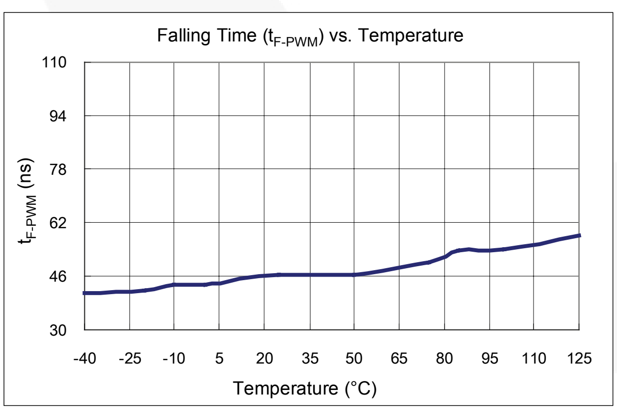

Figure 21. OPWM Falling Time

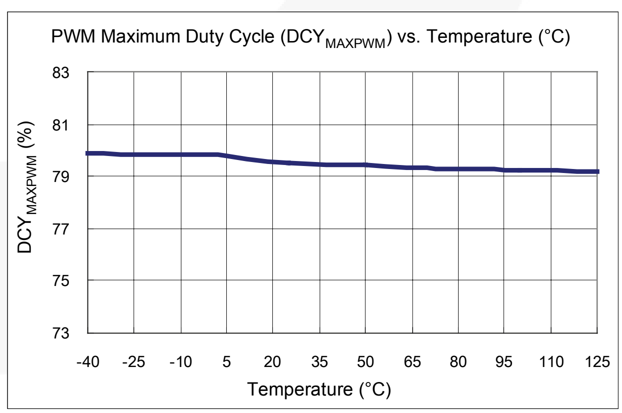

Figure 22. PWM Maximum Duty Cycle

Typical Performance Characteristics

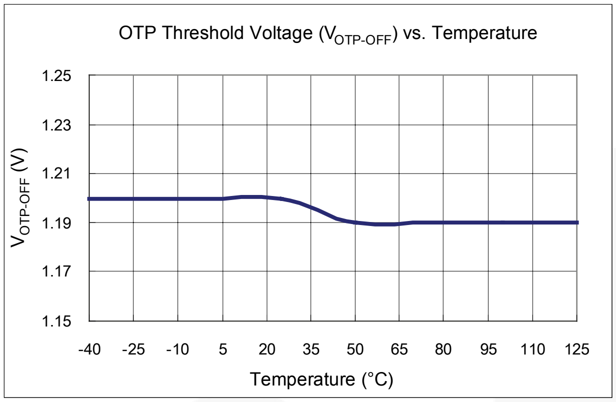

Figure 23.V_{DD} OTPurn Threshold Voltage

Functional Description

SG6901A is a highly integrated PFC/PWM combination controller. Many functions and protections are built in to provide a compact design. The following sections describe the operation and function.

Switching Frequency and Current Sources

The switching frequency can be programmed by the resistor RI connected between RI pin and GND. The relationship is:

$$f_{OSC} = \frac{1560}{R_I\ (k\Omega)}(kHz) \quad (1)$$

For example, a 24KΩ resistor R_I results in a 65KHz switching frequency. Accordingly, a constant current, I_T, flows through R_I:

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \quad (2)$$

I_T is used to generate internal current reference.

Line Voltage Detection (VRMS)

Figure 24 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The VRMS voltage is used for the PFC multiplier, brownout protection, and range control.

For brownout protection, SG6901A is disabled with a 195ms delay if the voltage VRMS drops below 0.8V.

For PFC multiplier and range control, refer to the PFC Operation section below for details.

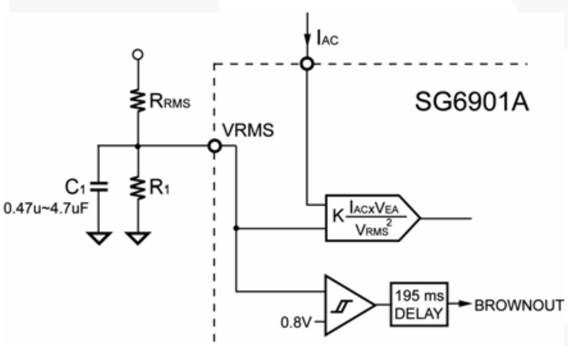

Figure 24.Line Voltage Detection Circuit

Interleave Switching

The SG6901A uses interleaved switching to synchronize the PFC and flyback stages, which reduces switching noise and spreads the EMI emissions. Figure 25 shows off-time, t_{OFF}, inserted between the turn-off of the PFC gate drive and the turn-on of the PWM.

For an universal input (90 ~ 264V_{AC}) power supply applying active boost PFC and flyback as a second stage, the output voltage of PFC is usually designed around 250V at low line and 390V at high line. This can improve the efficiency at low-line input. The RANGE pin (open-drain structure) is used for the two-level output voltage setting.

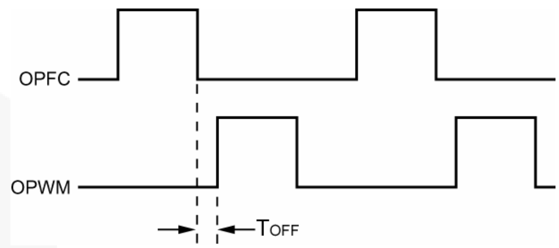

Figure 25.Interleaved Switching Pattern

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching charge multiplier-divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 26 shows the total control loop for the average-current-mode control circuit.

The current source output from the switching charge multiplier-divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^{2}}(\mu A) \quad (3)$$

As shown in Figure 26, the current output from the IMP pin is the summation of IMO and IMR1. IMR1 and IMR2 are identical fixed-current sources used to pull high the operating point of the IMP and IPFC pins since the voltage across RS goes negative with respect to ground. Constant current sources IMR1 and IMR2 are typically 60μA.

Through the differential amplification of the signal across R_S, better noise immunity is achieved. The output of IEA is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current I_S is proportional to IMO:

$$I_{MO} \times R_2 = I_S \times R_S \quad (4)$$

According to Equation 4, the minimum value of R_2 and maximum of R_S can be determined since IMO should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor R_S. The value of R_S should be small enough to reduce power consumption, but large enough to maintain the resolution. A current transformer (CT) may be used to improve efficiency of high-power converters.

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To achieve good power factor, the voltage for V_{RMS} and V_{EA} should be kept as constant as possible, according to Equation 5. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance ZO and a capacitor C_{EA} (1µF ~ 10µF) should be connected to ground. This establishes a dominant pole f1 for the voltage loop:

$$f_1 = \frac{1}{2\pi \times Z_O \times C_{EA}} \quad (5)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= V_{IN(rms)} \times I_{IN(rms)} \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \\ &= \sqrt{2} \times \frac{V_{EA}}{R_{AC}} \end{aligned} \quad (6)$$

From Equation 6, V_{EA}, the output of the voltage error amplifier, controls the total input power and the power delivered to the load.

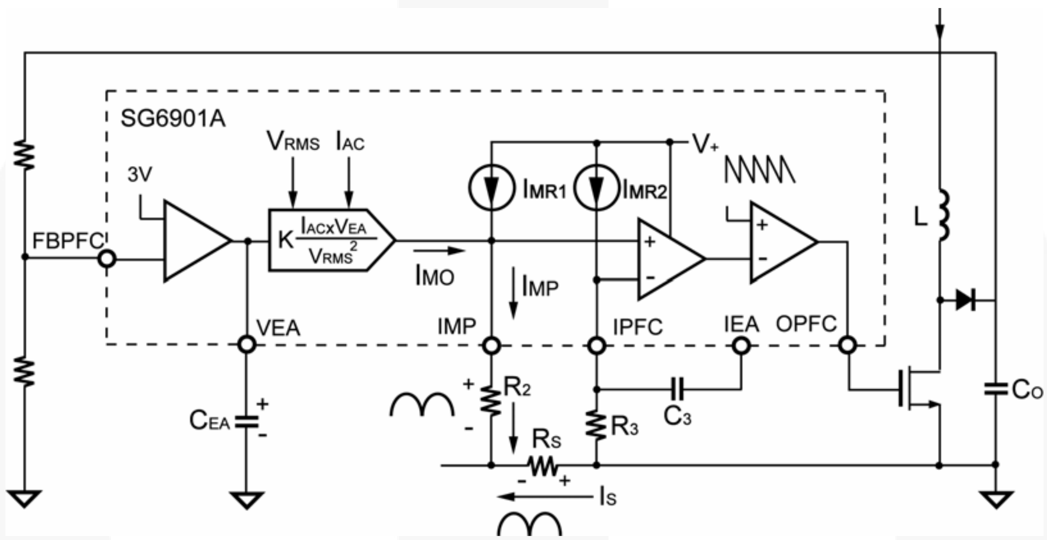

Figure 26. Average-Current-Mode Control Loop

Multi-Vector Error Amplifier

Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage.

0 shows the block diagram of the multi-vector error amplifier. When the variation of the feedback voltage exceeds ±5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response.

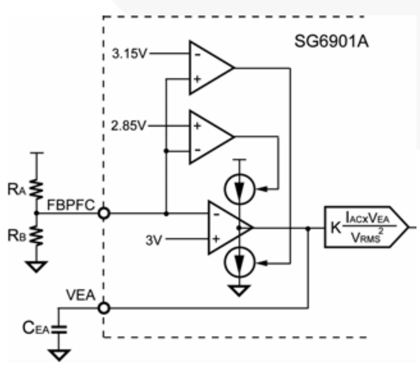

Figure 27. Multi-Vector Error Amplifier

PFC Over-Voltage Protection

Using a voltage divider from the output of PFC to the OVP pin, the PFC output voltage can be safely protected. Once the voltage on the OVP pin is over OVPPFC, the OPFC is disabled. THE OPFC is not enabled again until the OVP voltage falls below OVPPFC.

Cycle-by-Cycle Current Limiting

SG6901A provides cycle-by-cycle current limiting for both PFC and PWM stages. Figure 28 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on the ISENSE pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and V_{RMS} is shown in Figure 28.

The amplitude of the constant current, I_p, is determined by the internal current reference according to:

$$I_P = 2 \times \frac{1.2V}{R_I} \quad (8)$$

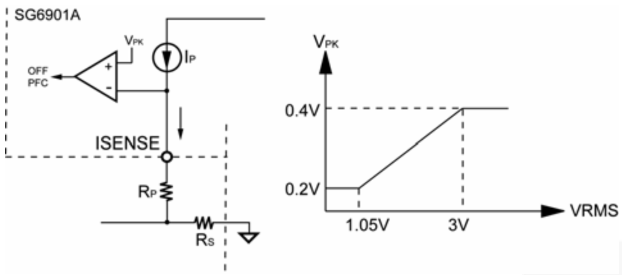

Figure 28. V_{RMS} Controlled Current Limiting

The peak current of the ISENSE is given by (V_{RMS}<1.05V):

$$I_{SENSE\_peak} = \frac{(I_P \times R_P) - 0.2V}{R_S} \quad (8)$$

Flyback PWM and Slope Compensation

As shown in Figure 29, peak-current-mode control is utilized for flyback PWM. The SG6901A inserts a synchronized 0.5V ramp at the beginning of each switching cycle. This built-in slope compensation ensures stable operation for continuous current-mode operation.

When the IPWM voltage, across the sense resistor, reaches the threshold voltage (0.9V), the OPWM is turned off after a small propagation delay t_{PD-PWM}.

To improve stability or prevent sub-harmonic oscillation, a synchronized positive-going ramp is inserted at every switching cycle.

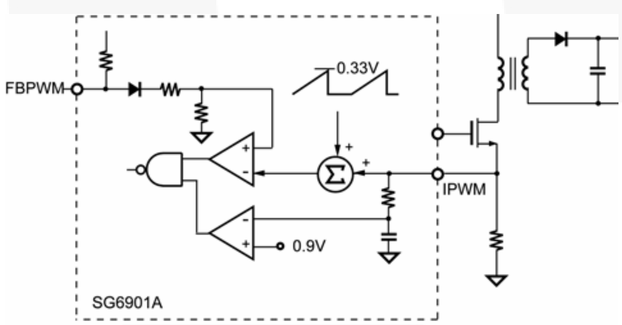

Figure 29. Peak Current Control Loop

Limited Power Control

Every time the output of the power supply is shorted or overloaded, the FBPWM voltage increases. If the FBPWM voltage is higher than a designed threshold, FBOPEN-LOOP (4.5V) for longer than $t_{OPEN-PWM}$ (56ms), the OPWM is turned off.

As long as the voltage on the VDD pin is larger than V_{DD-OFF} (minimum operating voltage), the OPWM is not enabled. This protection is reset every $t_{OPEN-PWM-Hiccup}$ interval. A low-frequency hiccup mode protection prevents the power supply from being overheated under overload conditions.

Over-Temperature Protection

The OTP pin provides for over-temperature protection. A constant current is output from this pin. If R_I is equal to 24KΩ, the magnitude of the constant current is 100μA. An external NTC thermistor must be connected from this pin to ground, as shown as Figure 30. When the OTP voltage drops below $V_{OTP-OFF}$ (1.2V), SG6901A is disabled and does not recover until OTP voltage exceeds V_{OTP-ON} (1.4V).

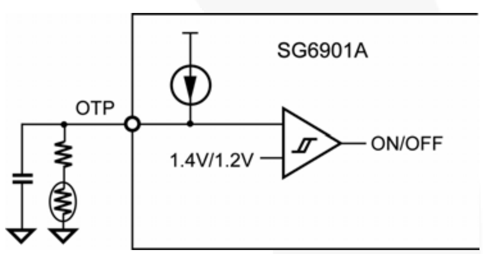

Figure 30. OTP Function

Soft Start

During startup of PWM stage, the SS pin charges an external capacitor with a constant current source. The voltage on FBPWM is clamped by the SS voltage during startup. In the event of a protected condition and/or PWM is disabled, the SS pin quickly discharges.

Gate Driver

SG6901A output stage is a fast totem-pole gate driver. The output driver is clamped by an internal 18V Zener diode to protect the external power MOSFET.

Physical Dimensions

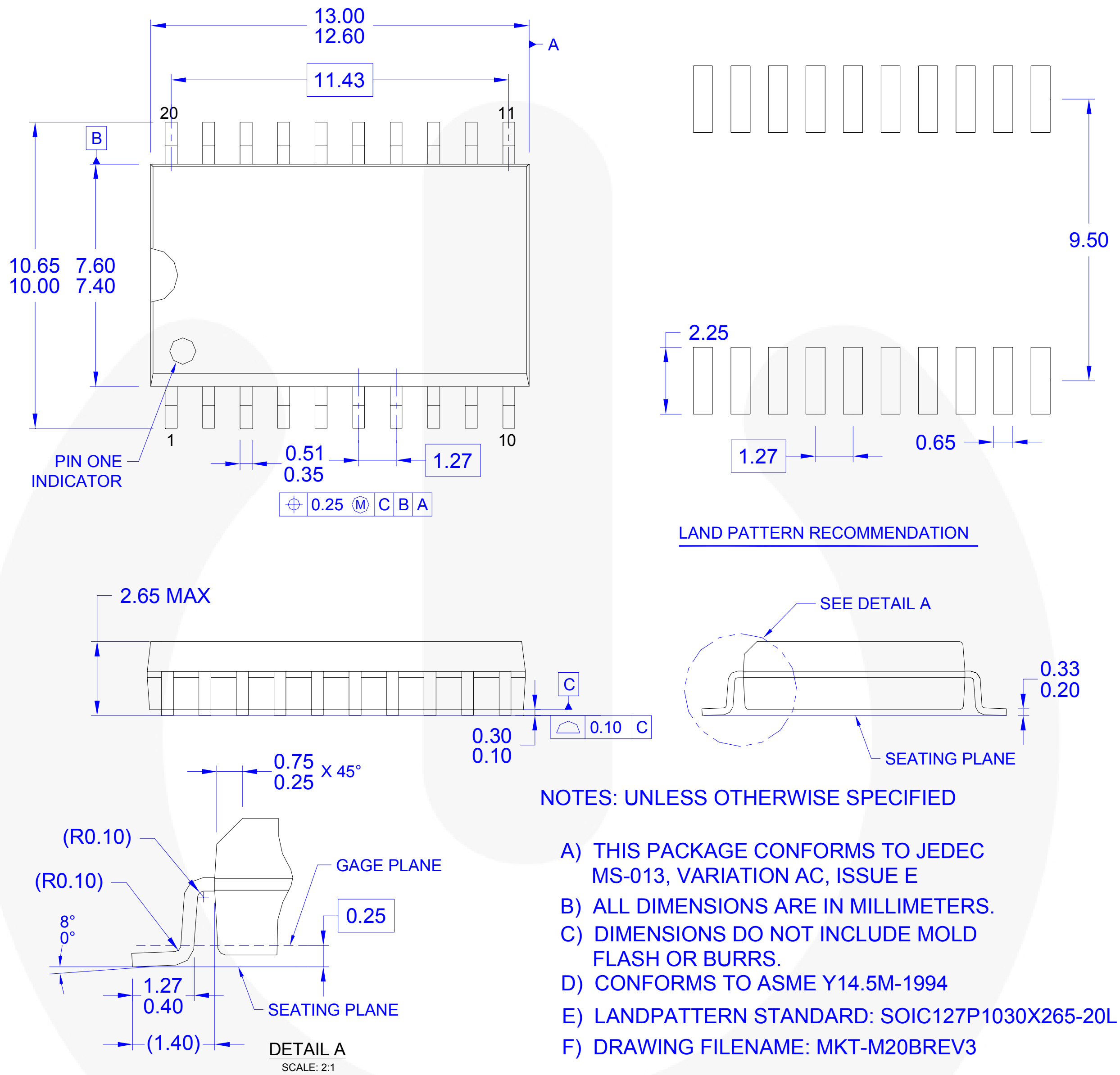

Figure 31. 20-Pin Small Outline Integrated Circuit (SOIC)

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