

# BLF25M612G

Power LDMOS transistor

Rev. 1 — 5 June 2012

Objective data sheet

## 1. Product profile

### 1.1 General description

12 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF25M612G is a driver designed for high power CW applications and is assembled in a high performance ceramic package.

**Table 1. Typical performance**

*RF performance at  $T_{case} = 25\text{ °C}$  in a common source class-AB production test circuit.*

Test signal	f (MHz)	$V_{DS}$ (V)	$P_{L(AV)}$ (W)	$G_p$ (dB)	$\eta_D$ (%)
CW	2450	28	12	18	58

### 1.2 Features and benefits

- High efficiency
- High power gain
- Excellent ruggedness
- Excellent thermal stability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

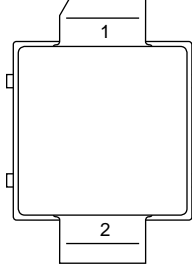
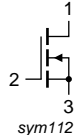
### 1.3 Applications

- Industrial, scientific and medical applications in the frequency range 2400 MHz to 2500 MHz



## 2. Pinning information

**Table 2. Pinning**

Pin	Description	Simplified outline	Graphic symbol
1	drain		
2	gate		
3	source		

[1] Connected to flange.

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
BLF25M612G	-	earless flanged ceramic package; 2 leads	SOT975C

## 4. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+13	V
$T_{stg}$	storage temperature		-65	-	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; P_L = 12\text{ W}$	4.0	K/W

## 6. Characteristics

**Table 6. Characteristics**

$T_j = 25\text{ °C}$  per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.18\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 18\text{ mA}$	1.4	1.9	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	3.2	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 0.9\text{ A}$	-	1.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 0.6\text{ A}$	-	0.8	1.3	$\Omega$

**Table 7. Application information**

Test signal: CW at  $f = 2450\text{ MHz}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 10\text{ mA}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 12\text{ W}$	17	18	-	dB
$RL_{in}$	input return loss	$P_L = 12\text{ W}$	-	-14	-10	dB
$\eta_D$	drain efficiency	$P_L = 12\text{ W}$	53	58	-	%

## 7. Test information

### 7.1 Ruggedness in class-AB operation

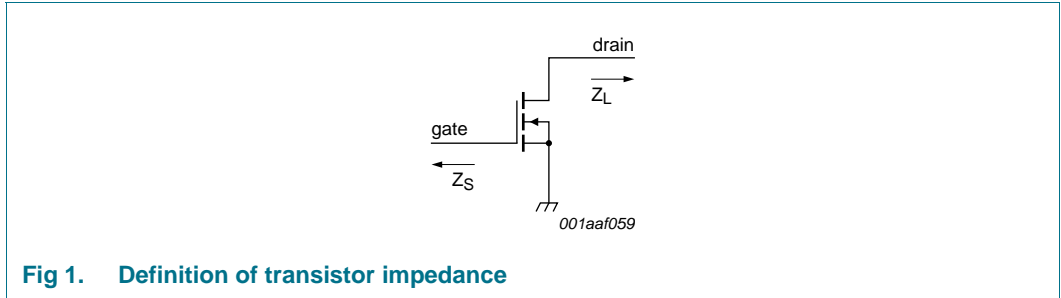
The BLF25M612G is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 28\text{ V}; I_{Dq} = 10\text{ mA}; P_L = 12\text{ W}$  (CW);  $f = 2450\text{ MHz}$ .

### 7.2 Impedance information

**Table 8. Typical impedance**

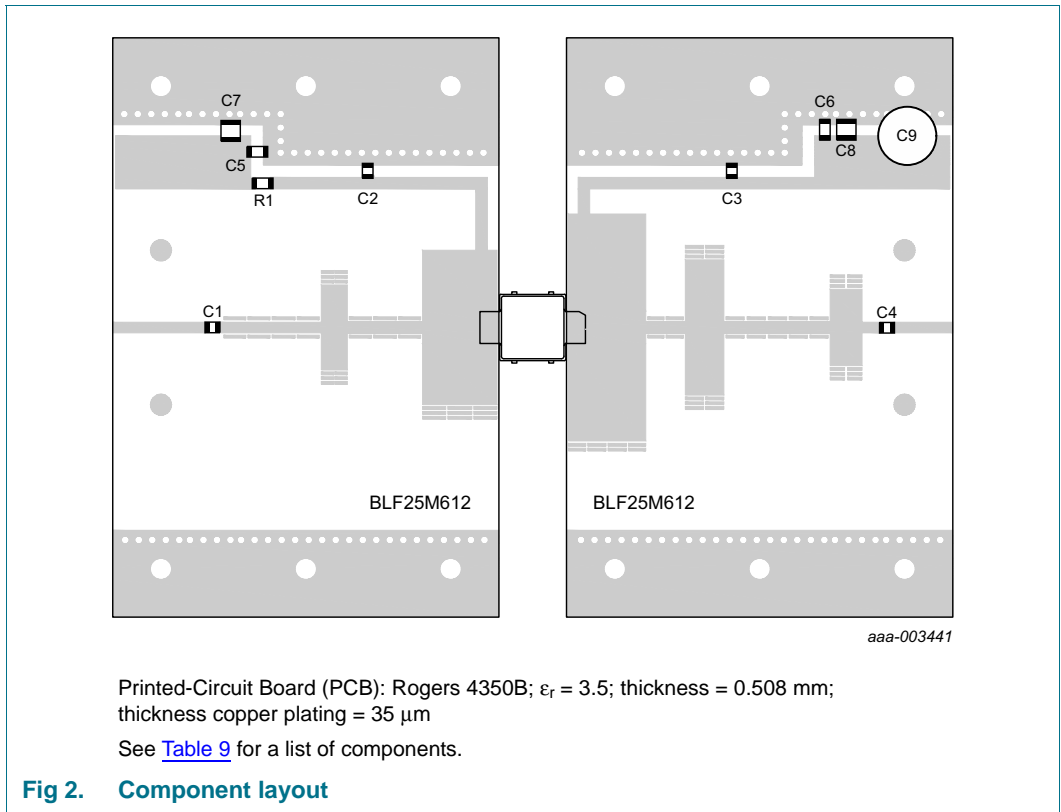
Measured load-pull data. Typical values unless otherwise specified.

f (MHz)	$Z_S$ ( $\Omega$ )	$Z_L$ ( $\Omega$ )
2400	3.0 – 11.4j	4.17 – 3.3j
2450	3.7 – 11.4j	4.3 – 2.7j
2500	3.8 – 11.4j	4.7 – 4.6j



**Fig 1. Definition of transistor impedance**

**7.3 Test circuit**



Printed-Circuit Board (PCB): Rogers 4350B;  $\epsilon_r = 3.5$ ; thickness = 0.508 mm; thickness copper plating = 35  $\mu\text{m}$

See [Table 9](#) for a list of components.

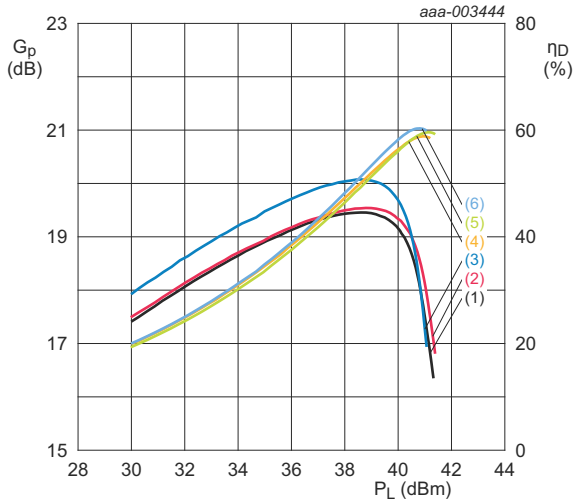
**Fig 2. Component layout**

**Table 9. List of components**

For test circuit see [Figure 2](#).

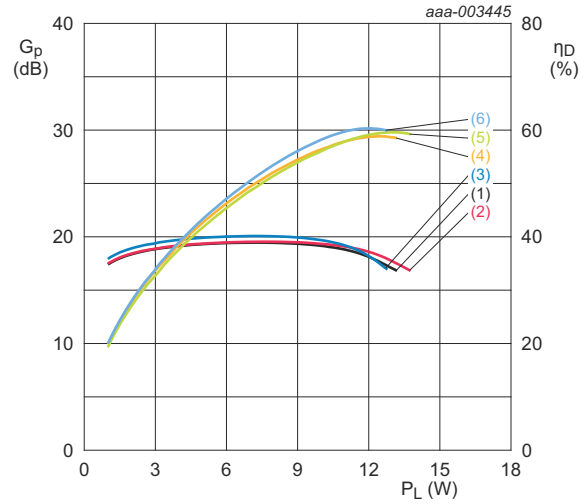
Component	Description	Value	Remarks
C1, C2, C3, C4	multilayer ceramic chip capacitor	15 pF	ATC100A
C5, C6	multilayer ceramic chip capacitor	220 nF	SMD 1206
C7, C8	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ ; 50 V	
C9	electrolytic capacitor	100 $\mu\text{F}$ ; 63 V	
R1	SMD resistor	7.5 $\Omega$	SMD 0805

7.4 Graphical data



- $V_{DS} = 28\text{ V}; I_{Dq} = 10\text{ mA}.$
- (1)  $G_p$  at  $f = 2400\text{ MHz}$
  - (2)  $G_p$  at  $f = 2450\text{ MHz}$
  - (3)  $G_p$  at  $f = 2500\text{ MHz}$
  - (4)  $\eta_D$  at  $f = 2400\text{ MHz}$
  - (5)  $\eta_D$  at  $f = 2450\text{ MHz}$
  - (6)  $\eta_D$  at  $f = 2500\text{ MHz}$

Fig 3. Power gain and drain efficiency as function of load power; typical values



- $V_{DS} = 28\text{ V}; I_{Dq} = 10\text{ mA}.$
- (1)  $G_p$  at  $f = 2400\text{ MHz}$
  - (2)  $G_p$  at  $f = 2450\text{ MHz}$
  - (3)  $G_p$  at  $f = 2500\text{ MHz}$
  - (4)  $\eta_D$  at  $f = 2400\text{ MHz}$
  - (5)  $\eta_D$  at  $f = 2450\text{ MHz}$
  - (6)  $\eta_D$  at  $f = 2500\text{ MHz}$

Fig 4. Power gain and drain efficiency as function of load power; typical values

## 8. Package outline

Earless flanged ceramic package; 2 leads

SOT975C

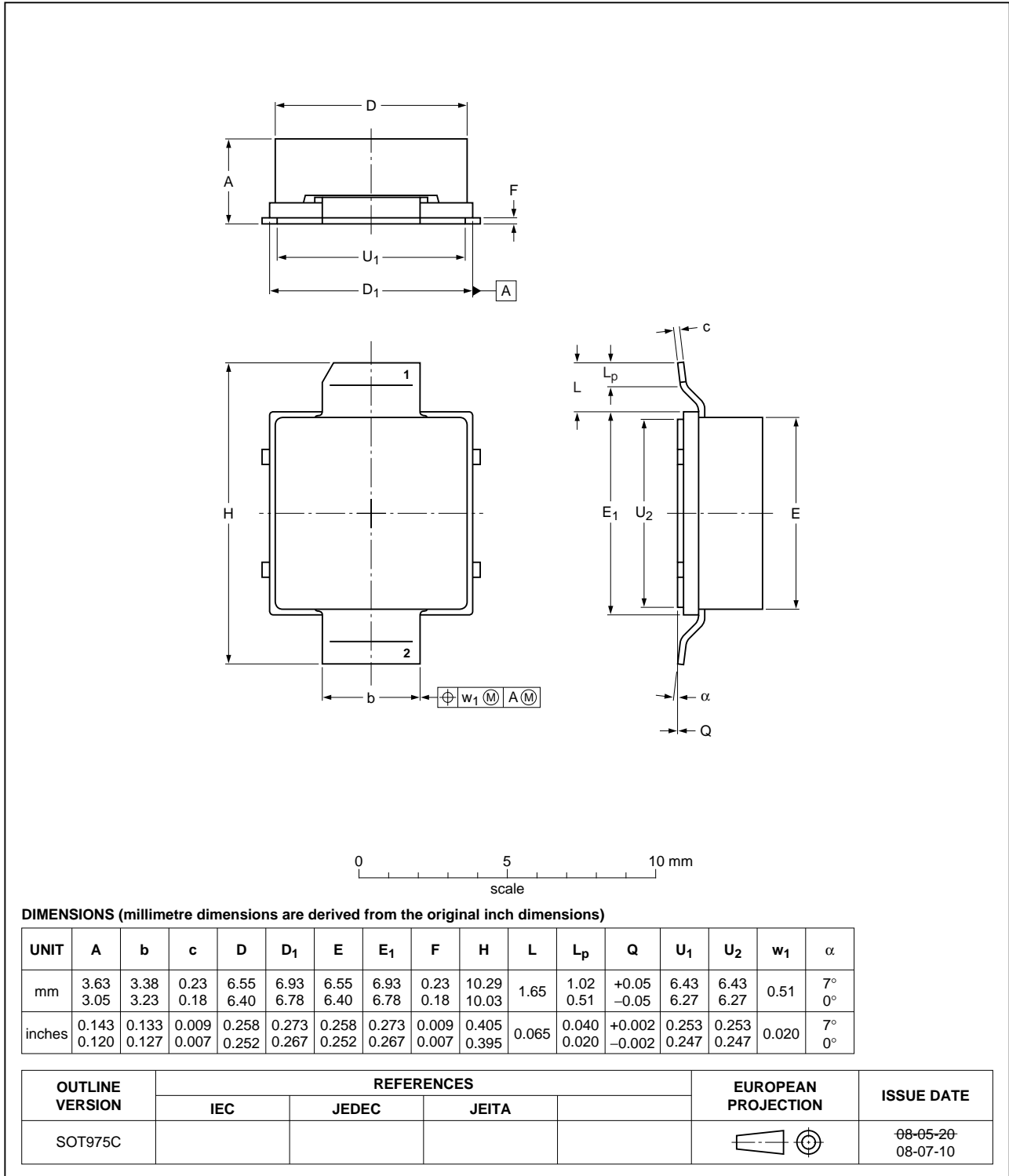


Fig 5. Package outline SOT975C

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF25M612G v.1	20120605	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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