NTF3055L108, NVF3055L108

Power MOSFET

3.0 A, 60 V, Logic Level, N−Channel SOT−223

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- AEC Q101 Qualified − NVF3055L108
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Drain−to−Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	60	Vdc
Gate−to−Source Voltage − Continuous − Non−repetitive ($t_p \le 10$ ms)	V_{GS}	 ± 15 ± 20	 Vdc Vpk
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 100°C − Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 3.0 1.4 9.0	Adc Apk
Total Power Dissipation @ T_A = 25°C (Note 1) Total Power Dissipation @ T_A = 25°C (Note 2) Derate above 25°C	P_D	2.1 1.3 0.014	Watts Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to 175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 25 Vdc, V_{GS} = 5.0 Vdc, $I_{L(pk)}$ = 7.0 Apk, L = 3.0 mH, V_{DS} = 60 Vdc)	E_{AS}	74	mJ
Thermal Resistance −Junction−to−Ambient (Note 1) −Junction−to−Ambient (Note 2)	 $R_{\theta JA}$ $R_{\theta JA}$	 72.3 114	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. When surface mounted to an FR4 board using 1″ pad size, 1 oz. (Cu. Area 0.0995 in^2).
2. When surface mounted to an FR4 board using minimum recommended pad size, 2−2.4 oz. (Cu. Area 0.272 in^2).

ON Semiconductor®

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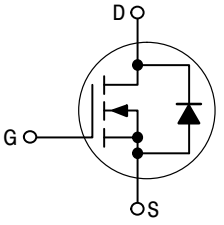
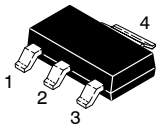
3.0 A, 60 V

$R_{DS(on)}$ = 120 mΩ

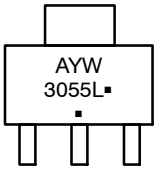
N−Channel





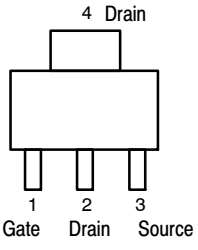
SOT−223
CASE 318E
STYLE 3

MARKING DIAGRAM



3055L = Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 3) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 –	 68 68	 – –	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 – –	 – –	 1.0 10	μAdc
Gate−Body Leakage Current	(V_{GS} = ± 15 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	–	–	± 100	nAdc
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage (Note 3) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 –	 1.68 4.6	 2.0 –	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 1.5 Adc)		$R_{DS(on)}$	–	92	120	mΩ
Static Drain−to−Source On−Resistance (Note 3) (V_{GS} = 5.0 Vdc, I_D = 3.0 Adc) (V_{GS} = 5.0 Vdc, I_D = 1.5 Adc, T_J = 150°C)		$V_{DS(on)}$	–	 0.290 0.250	 0.43 –	Vdc
Forward Transconductance (Note 3)	(V_{DS} = 7.0 Vdc, I_D = 3.0 Adc)	g_{fs}	–	5.7	–	Mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 V, f = 1.0 MHz)	C_{iss}	–	313	440	pF
Output Capacitance		C_{oss}	–	112	160	
Transfer Capacitance		C_{rss}	–	40	60	
SWITCHING CHARACTERISTICS (Note 4)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 3.0 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 3)	$t_{d(on)}$	–	11	25	ns
Rise Time		t_r	–	35	70	
Turn−Off Delay Time		$t_{d(off)}$	–	22	45	
Fall Time		t_f	–	27	60	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 3.0 Adc, V_{GS} = 5.0 Vdc) (Note 3)	Q_T	–	7.6	15	nC
		Q_1	–	1.4	–	
		Q_2	–	4.0	–	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 3.0 Adc, V_{GS} = 0 Vdc) (I_S = 3.0 Adc, V_{GS} = 0 Vdc, T_J = 150°C) (Note 3)	V_{SD}	 – –	 0.87 0.72	 1.0 –	Vdc
Reverse Recovery Time	(I_S = 3.0 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 3)	t_{rr}	–	35	–	ns
		t_a	–	21	–	
		t_b	–	14	–	
Reverse Recovery Stored Charge		Q_{RR}	–	0.044	–	μC

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL ELECTRICAL CHARACTERISTICS

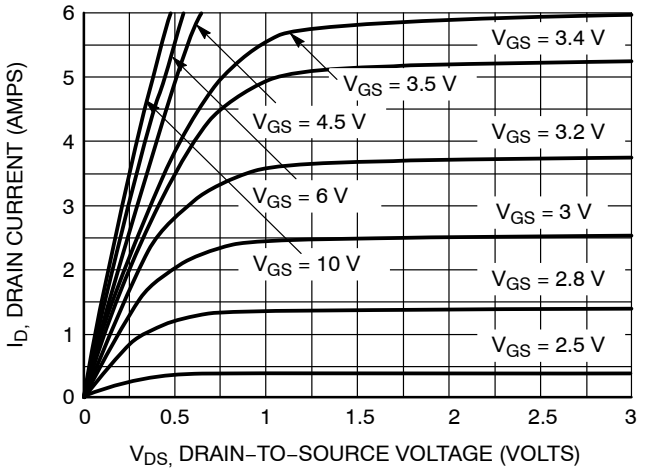


Figure 1. On−Region Characteristics

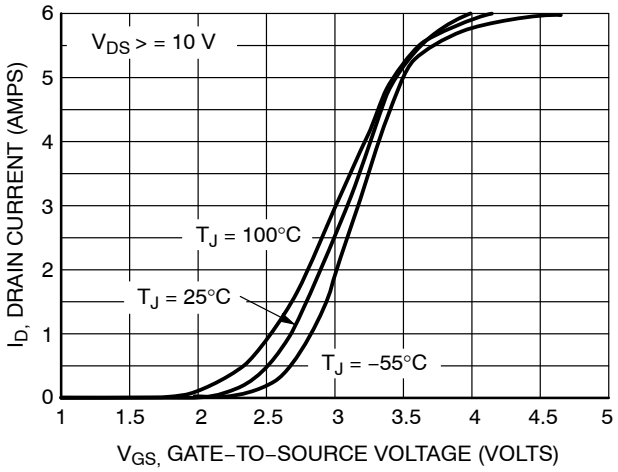


Figure 2. Transfer Characteristics

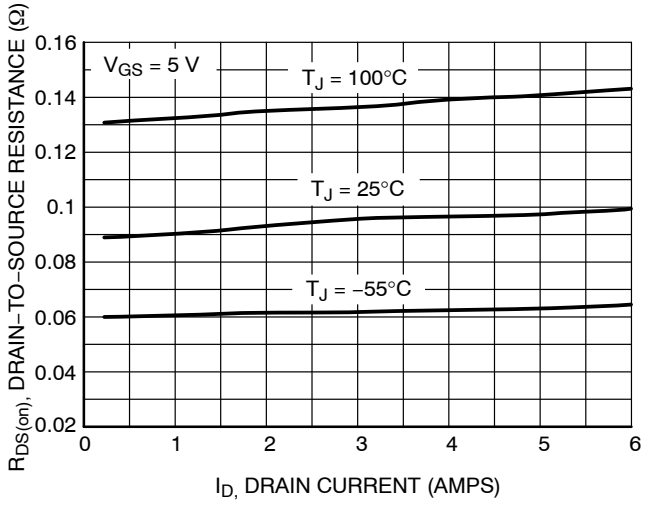


Figure 3. On−Resistance vs. Gate−to−Source Voltage

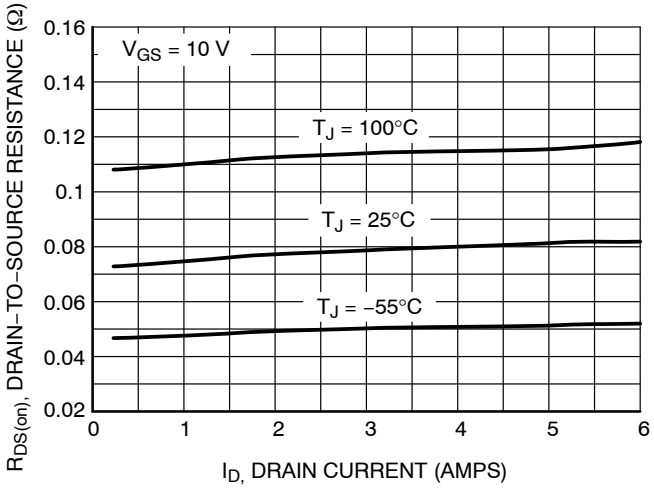


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

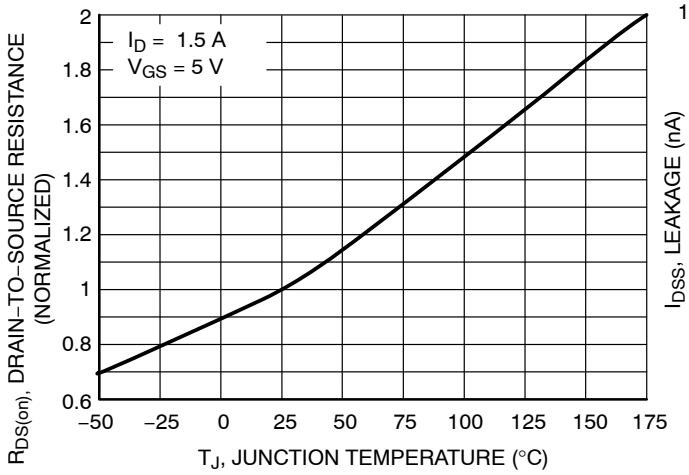


Figure 5. On−Resistance Variation with Temperature

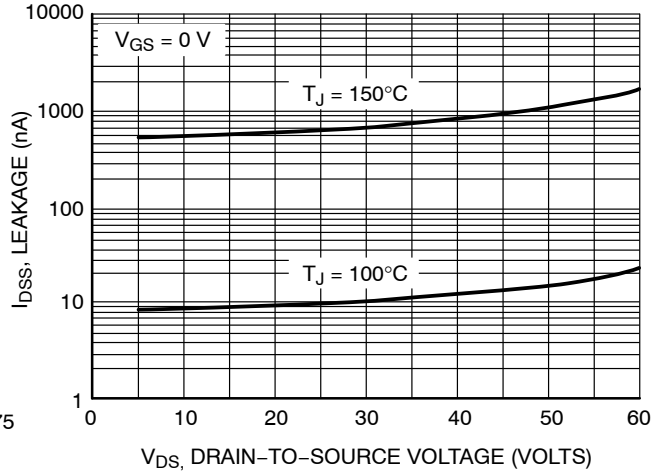


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL ELECTRICAL CHARACTERISTICS

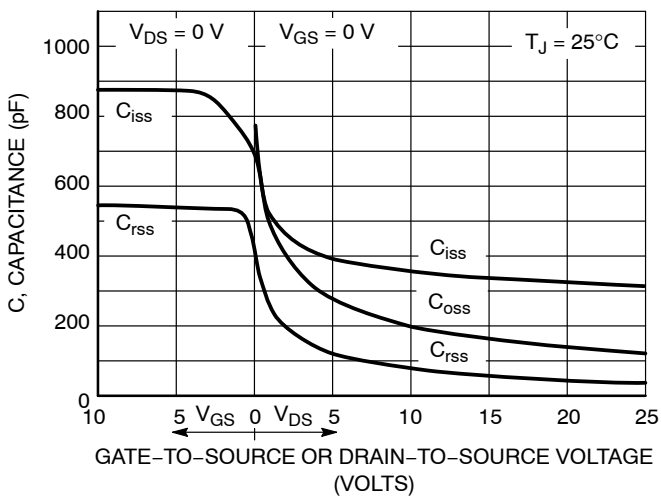


Figure 7. Capacitance Variation

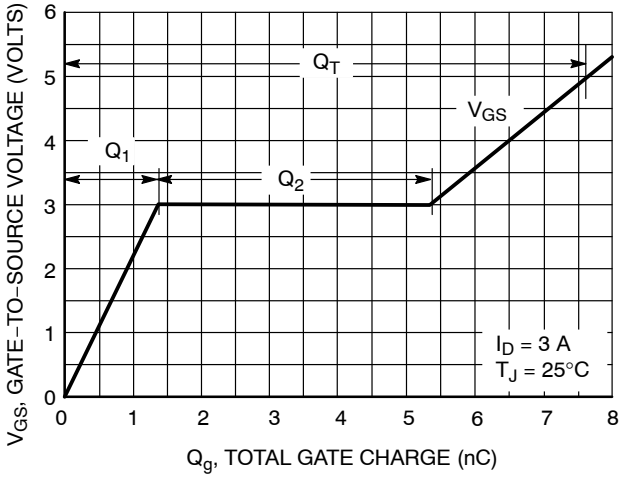


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

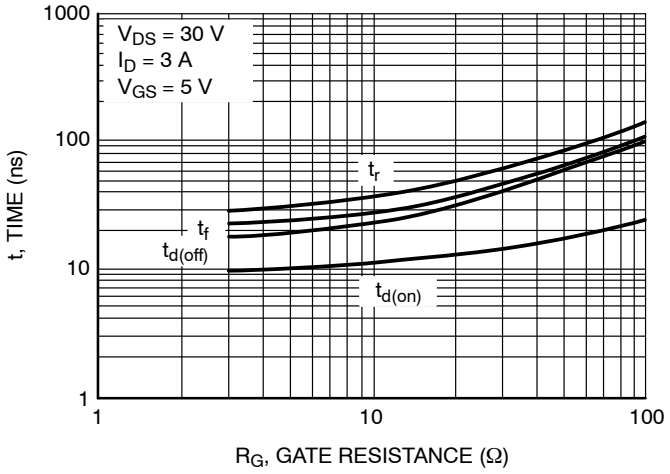


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

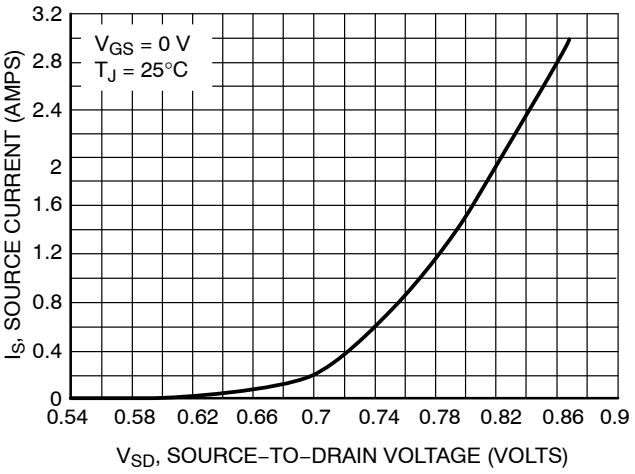


Figure 10. Diode Forward Voltage vs. Current

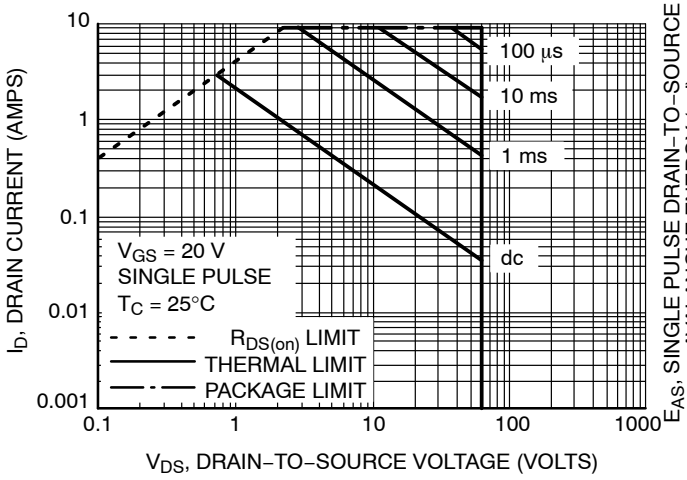


Figure 11. Maximum Rated Forward Biased Safe Operating Area

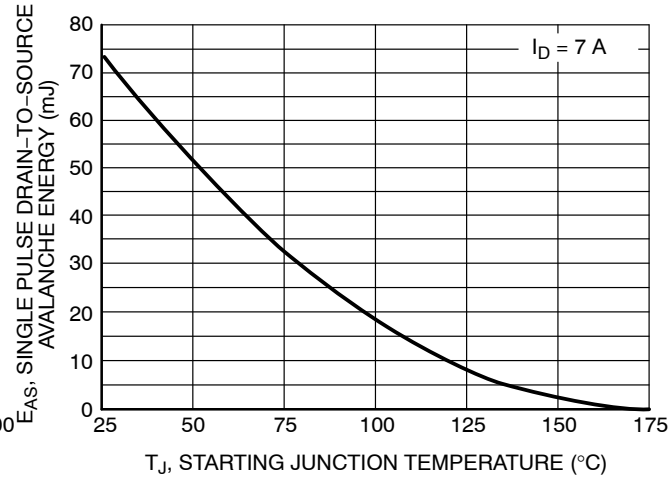


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

TYPICAL ELECTRICAL CHARACTERISTICS

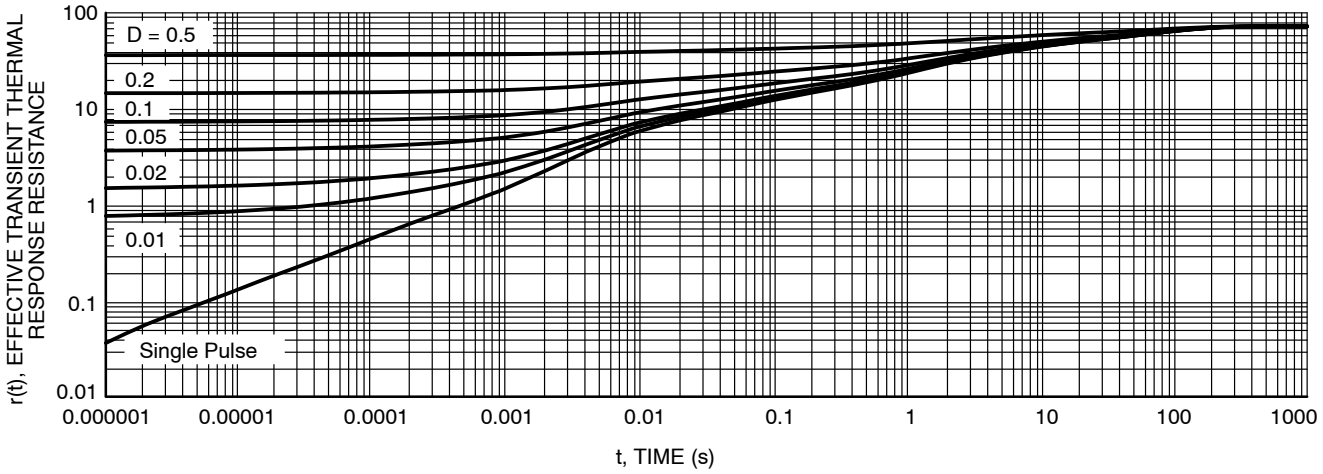


Figure 13. Thermal Response

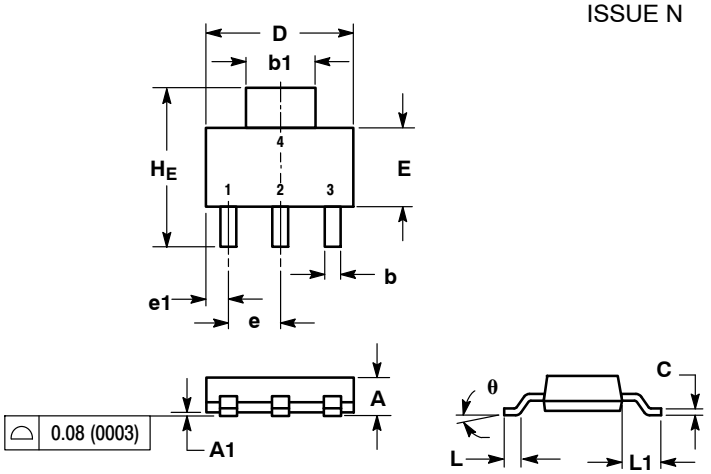
ORDERING INFORMATION

Device	Package	Shipping†
NTF3055L108T1G	SOT−223 (TO−261) (Pb−Free)	1000 / Tape & Reel
NVF3055L108T1G	SOT−223 (TO−261) (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

SOT−223 (TO−261)
CASE 318E−04
ISSUE N

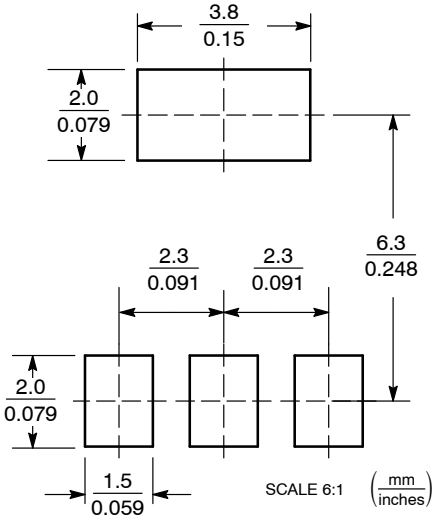


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	−−−	−−−	0.008	−−−	−−−
L1	1.50	1.75	2.00	0.060	0.069	0.078
H_E	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	–	10°	0°	–	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
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