# AOZ2002

## 2A Ultra Low Dropout Linear Regulator

## General Description

The AOZ2002 is a 2A ultra low dropout linear regulator designed for desktop motherboard, graphic card and notebook applications. This device needs dual supplies, a control voltage for the control circuitry and an input voltage for power conversion. The AOZ2002 delivers high-current and ultra low-drop output voltage for applications where $V_{OUT}$ is very close to $V_{IN}$.

The AOZ2002 features comprehensive control and protection functions: a power on reset (POR) circuit for monitoring both control and power inputs for proper operation; an EN input for enabling or disabling the device, a power OK with time delay for indicating the output voltage status, a current limit function, and a thermal shutdown function.

The AOZ2002 is available in exposed pad SO-8 package.

## Features

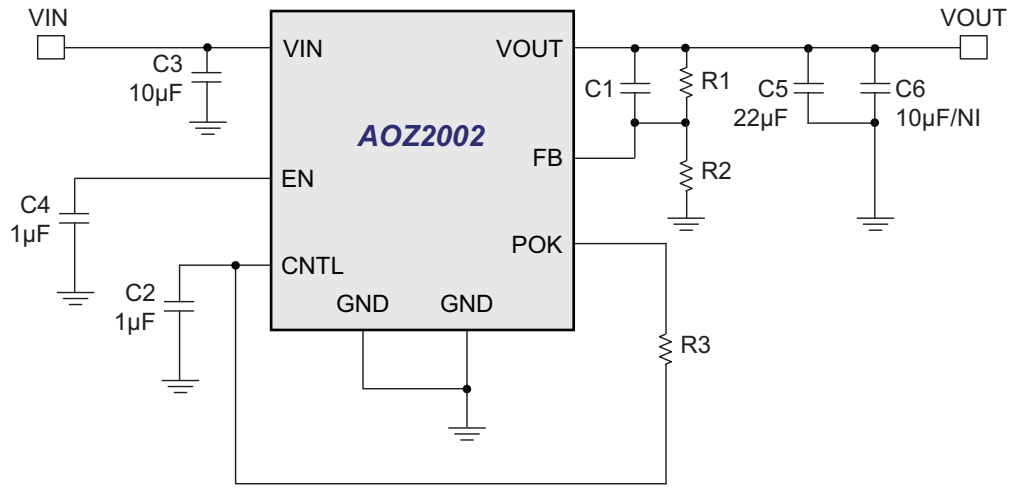
- Ultra low dropout linear regulator
- 1.3V~5.5V $V_{IN}$ supply voltage with external control voltage
- Dropout voltage (typical):
  - 90mV @ 1A
  - 180mV @ 2A
- High accuracy output voltage ±1.5%
- Enable and Power Good
- $V_{OUT}$ pull low resistance when disabled
- Current limiting protection
- Thermal shutdown protection
- Output voltage adjustable
- Small footprint exposed pad SO-8 Package

## Applications

- Desktop, notebook PCs
- Workstations
- Graphic cards
- Low voltage logic supplies
- Gaming
- SMPS post regulators

Green Product

## Typical Application

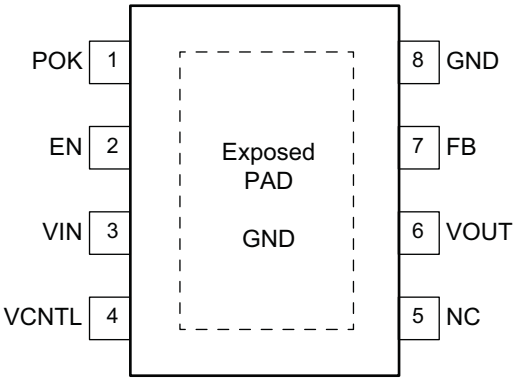


## Ordering Information

| Part Number | Ambient Temperature Range | Package | Environmental |
|---|---|---|---|
| AOZ2002PI | -40 °C to +85 °C | EPAD SO-8 | Green Product |

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/media/AOSGreenPolicy.pdf for additional information.

## Pin Configuration

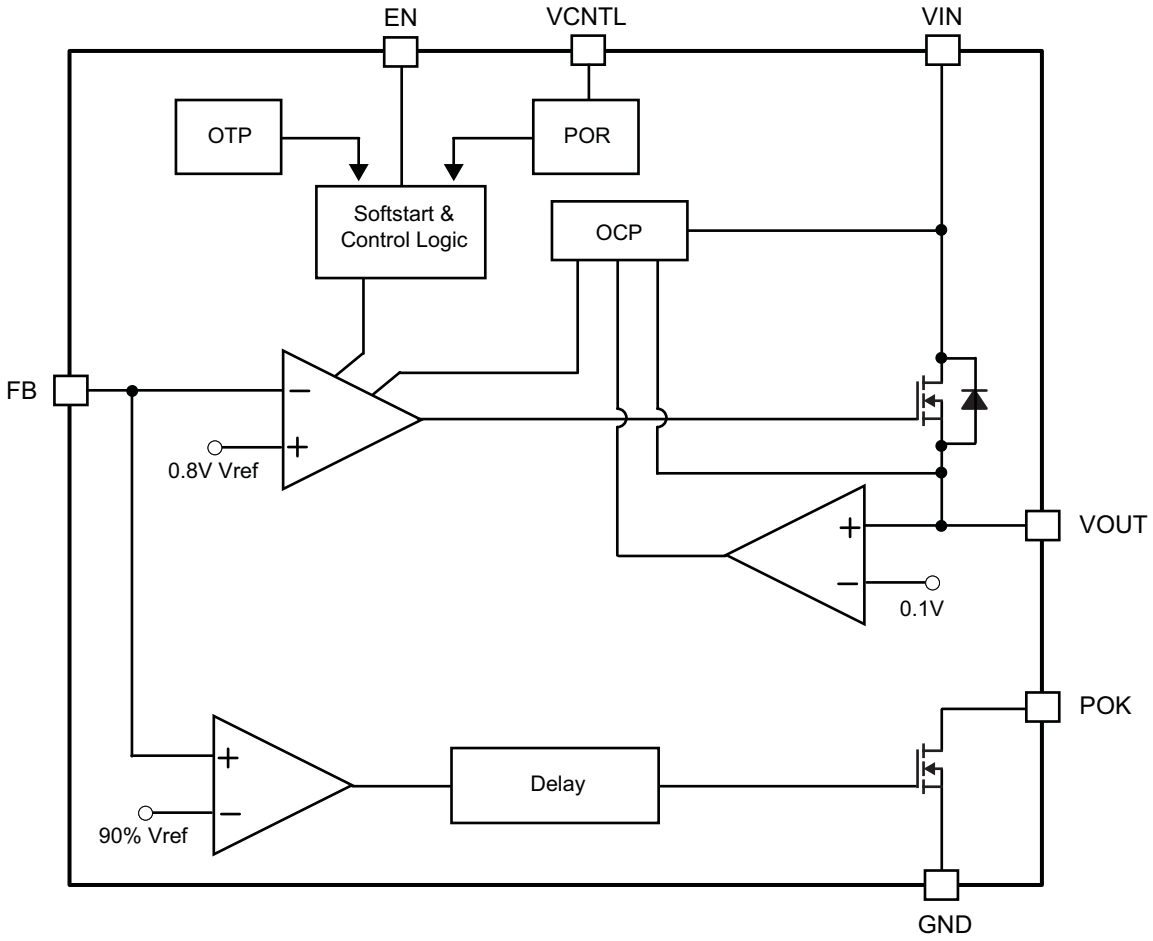



**EPAD SO-8**
**(Top View)**

## Pin Description

| Pin Number | Pin Name | Pin Function |
|---|---|---|
| 1 | POK | Power OK Indication. This pin is an open-drain output and is set high impedance once VOUT reaches 90% of its rating voltage. |
| 2 | EN | Enable Input. Pulling this pin below 0.8V turns the regulator off, reducing the quiescent current to a fraction of its operating value. |
| 3 | VIN | Input Voltage. This is the drain input to the power device that supply current to the output pin. Large bulk capacitors with low ESR should be placed physically close to this pin o prevent the input rail from dropping during large load transient. A 10µF ceramic capacitor is recommended at this pin. |
| 4 | VCNTL | Supply Input for Control Circuit. This pin provides bias voltage to the control circuitry and driver for the pass transistor. The driving capability of output current is proportioned to the VCNTL. For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, and no less than VCNTL_min. |
| 5 | NC | Not Internally Connected. |
| 6 | VOUT | Output Voltage. This pin is power output of the device. A pull low resistance exists when the device is disabled by pulling low the EN pin. |
| 7 | FB | Feedback Voltage. This pin is the inverting input to the error amplifier. A resistor divider from the output to GND is used to set the regulation voltage as VOUT=0.8x(R1+R2)/R2 (V). |
| 8 | GND | Ground. |
| Exposed PAD | GND | Ground. The exposed pad acts the dominant power dissipation path and should be soldered to well design PCB pads. |

## Block Diagram




## Absolute Maximum Ratings

*Exceeding the Absolute Maximum Ratings may damage the device.*

| Parameter | Rating |
|---|---|
| VIN | 1V to 6.5V |
| VCNTL | 3V to 6V |
| VOUT | 0.8V to 6V |
| Other Pins | -0.3V to 6V |
| ESD Rating(1) | 2kV |

**Note:**

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model rating: 1.5kΩ in series with 100pF.

## Recommended Operating Conditions

*The device is not guaranteed to operate beyond the Recommended Operating Conditions.*

| Parameter | Rating |
|---|---|
| Supply Voltage ($V_{IN}$) | 1.3V to 5.5V |
| Supply Control Voltage ($V_{CNTL}$) | 3V to 5.5V |
| Junction Temperature ($T_J$) | -40°C to +125°C |
| Ambient Temperature ($T_A$) | -40°C to +85°C |
| Power Dissipation ($P_D$) | 2W |
| Package Thermal Resistance EPAD SO-8 ($\Theta_{JA}$) | 50°C/W |

## Electrical Characteristics

$T_A$ = 25 °C, $V_{IN}$ = 1.4V, $V_{CNTL}$ = $V_{EN}$ = 5V, $C_{IN}$ = $C_{OUT}$ = 10µF, unless otherwise specified. Specifications in **BOLD** indicate a temperature of -40°C to +85°C.

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| **INPUT STAGE** | | | | | | |
| $V_{IN}$ | Input Voltage Range | $V_{OUT}$ = 1.2V, $I_{OUT}$ = 100mA | 1.3 | | 5.5 | V |
| $V_{CNTL}$ | Input Control Voltage | | 1.5 | | 5.5 | V |
| $V_{POR}$ | POR | | 2.4 | 2.7 | 3 | V |
| $V_{UVLO\_HYS}$ | Under-Voltage Lockout Hysteresis | | | 300 | | mV |
| $I_{CNTL}$ | Input Supply Current | EN = IN, $V_{OUT}$ = $V_{FB}$, no load | | 0.5 | 1 | mA |
| | | EN = AGND | | | 20 | µA |
| $V_{FB}$ | Feedback Reference Voltage | $T_A$ = 25 ºC, no load | 0.788 | 0.800 | 0.812 | V |
| $I_{FB}$ | Feedback Bias Current | | | 0.02 | | µA |
| **REGULATION** | | | | | | |
| $\Delta V_{FB}$ | Line Regulation ($V_{IN}$) | $V_{IN}$ = 1.4V to 5V, $I_{OUT}$ = 100mA, $V_{OUT}$ = 1.2 V | | 0.015 | 0.15 | % / ΔV |
| | Load Regulation | $V_{IN}$ = 1.8V, $I_{OUT}$ = 100mA to 2A, $V_{OUT}$ = 1.2V | | 0.45 | 1.5 | % |
| $V_{DROP}$[1] | Drop Voltage | $I_{OUT}$ = 300mA, $V_{EN}$ = $V_{CNTL}$ = 5V, $V_{OUT}$ = 1.2V | | 40 | 50 | mV |
| | | $I_{OUT}$ = 2A, $V_{EN}$ = $V_{CNTL}$ = 5V, $V_{OUT}$ = 1.2V | | 180 | 250 | mV |
| $R_{PULL-DOWN}$ | $V_{OUT}$ Pull-down | | | 90 | | Ω |
| **ENABLE / POK** | | | | | | |
| $V_{EN\_HI}$ | Enable High Level | | 1.2 | | | V |
| $V_{EN\_LOW}$ | Disable Low Level | | | | 0.2 | V |
| $I_{EN}$ | Enable Bias Current | $V_{EN}$ = 5.5V | | 12 | | µA |
| $V_{POK\_TH}$ | POK Threshold | $V_{IN}$ = $V_{EN}$ =$V_{CNTL}$ = 5V, No load, $V_{OUT}$ = 1.2V | | 90 | | % |
| $V_{POK\_HYS}$ | POK Hysteresis | $V_{IN}$ = $V_{EN}$ =$V_{CNTL}$ = 5V, No load, $V_{OUT}$ = 1.2V | | 10 | | % |
| $T_{POK\_ON}$ | POK Time Delay (ON) | $V_{IN}$ = $V_{EN}$ =$V_{CNTL}$ = 5V, No load, $V_{FB}$ > 90%*$V_{REF}$ | | 1 | | ms |
| $T_{POK\_OFF}$ | POK Time Delay (OFF) | $V_{IN}$ = $V_{EN}$ =$V_{CNTL}$ = 5V, No load, $V_{FB}$ < 10%*$V_{REF}$ | | 50 | | µs |
| $V_{POK\_LOW}$ | POK Pull-low Voltage | POK sink current = 5mA | | | 0.35 | V |
| **PROTECTION** | | | | | | |
| $I_{LIM}$[2] | Current Limit | | 2.2 | 2.7 | | A |
| $I_{SC}$ | Short Circuit Current | $V_{OUT}$ < 0.1V | | 0.8 | | A |
| $T_{SD}$ | Thermal Shutdown Threshold | | | 160 | | ºC |
| $\Delta T_{SD}$ | Thermal Shutdown Hysteresis | | | 30 | | ºC |
| | Thermal Shutdown Temperature Reset | $V_{OUT}$ < 0.1V | | 100 | | ºC |

**Note:**

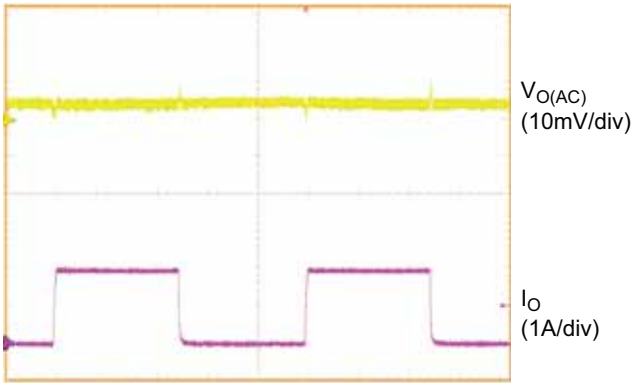
1. The dropout voltage is defined as $V_{IN}$ - $V_{OUT}$, which is measured when $V_{OUT}$ is $V_{OUT}$ - 100mV.
2. The current limit was measured by the constant current limit value when VOUT is shorted directly. It is noted that the output capacitor current was not included.

## Typical Performance Characteristics

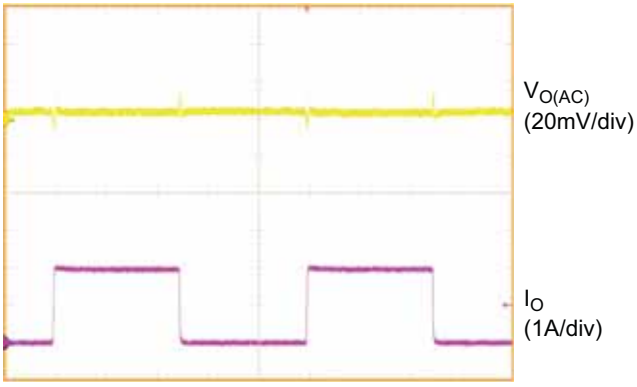
## Typical Performance Characteristics

Circuit of Typical Application 1. $T_A$ = 25°C, $V_{IN}$ = 1.5V, $V_{CNTL}$ = 5V, $V_{OUT}$ = 1.05V, unless otherwise specified.

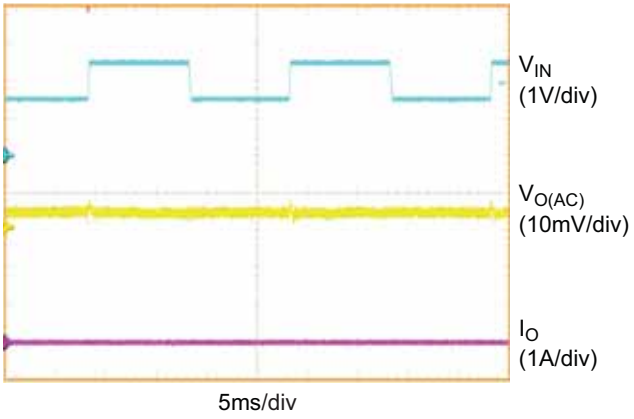
**Load Transient Response (1A)**



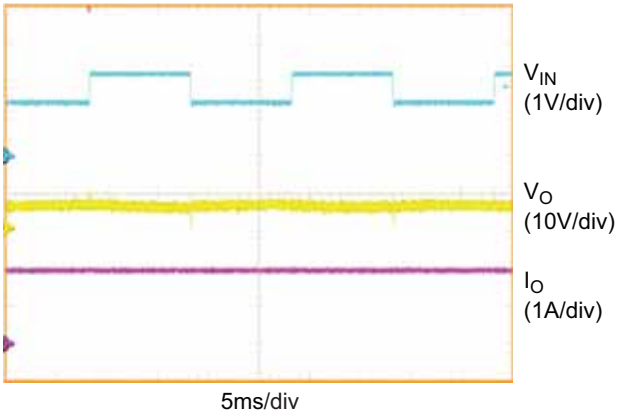

**Load Transient Response (2A)**



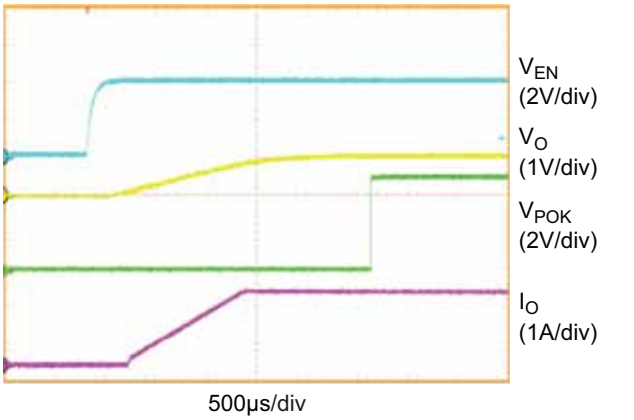

**$V_{IN}$ Line Transient Response (0A)**



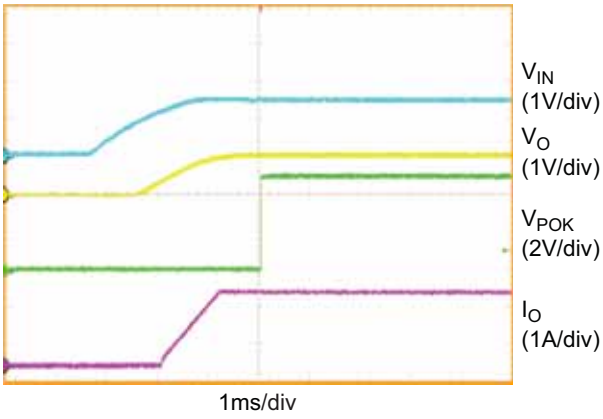

**$V_{IN}$ Line Transient Response (2A)**




**Start-Up From Enable**



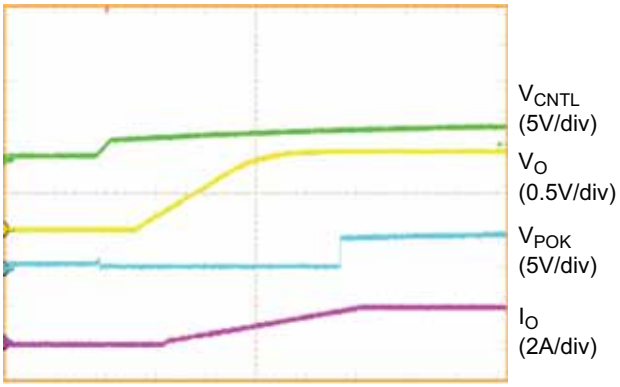

**Start-Up From $V_{IN}$**



## Typical Performance Characteristics *(Continued)*

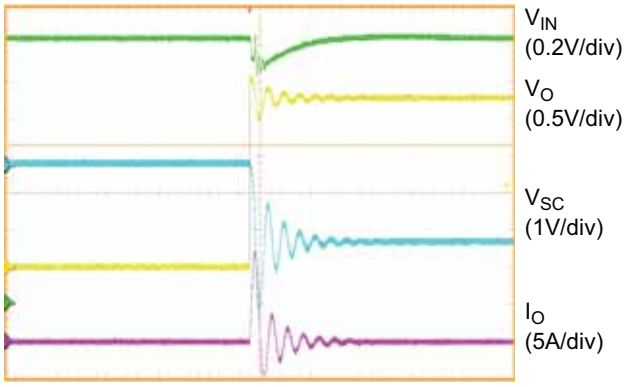
Circuit of Typical Application 1. $T_A$ = 25°C, $V_{IN}$ = 1.5V, $V_{CNTL}$ = 5V, $V_{OUT}$ = 1.05V, unless otherwise specified.

**Start-Up From $V_{CNTL}$**



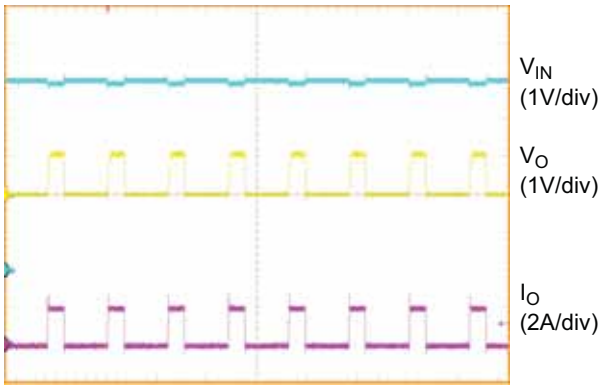

500µs/div

**Short Current Protection**



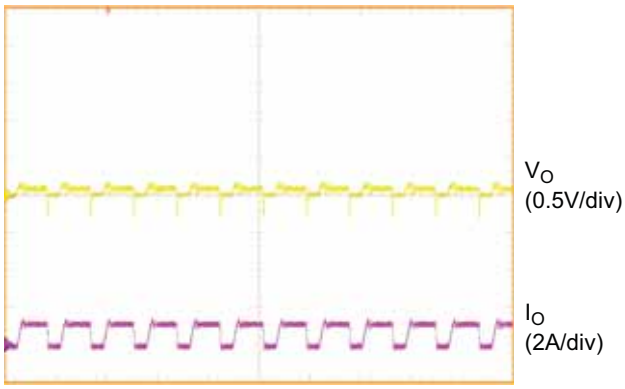

50µs/div

**Over Temperature Protection ($V_{IN}$ = 5V)**




20ms/div

**Current Limit**

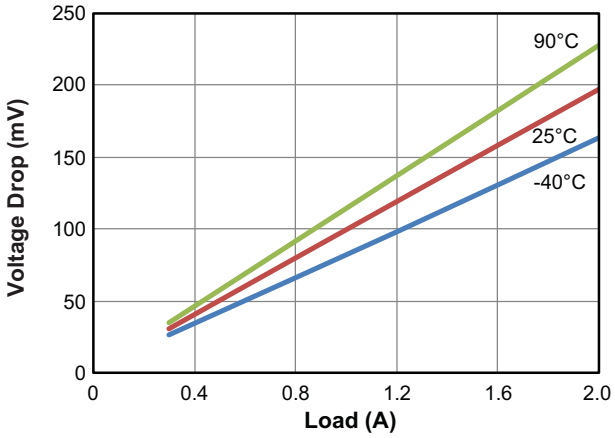



20ms/div

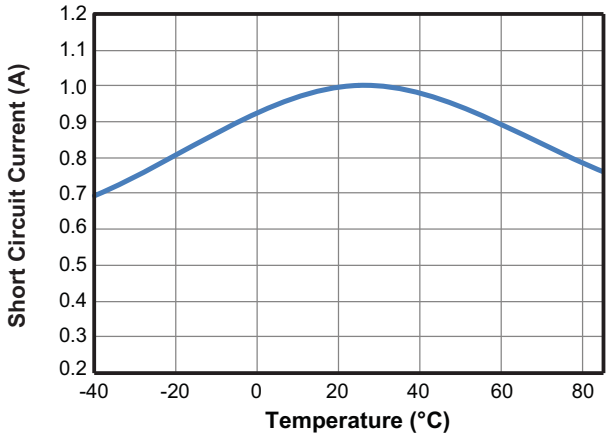
## Typical Performance Characteristics *(Continued)*

Circuit of Typical Application 1. $T_A$ = 25°C, $V_{IN}$ = 1.5V, $V_{CNTL}$ = 5V, $V_{OUT}$ = 1.05V, unless otherwise specified.

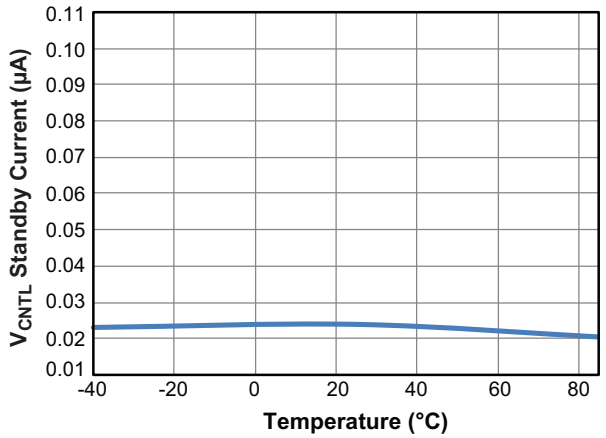
**Dropout Voltage vs. Load Current**



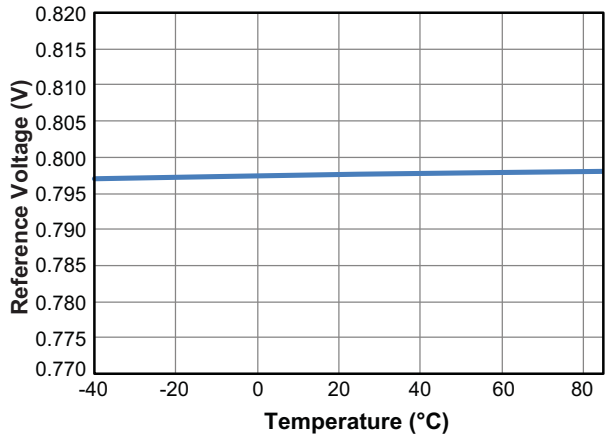

**Short Circuit vs. Temperature**



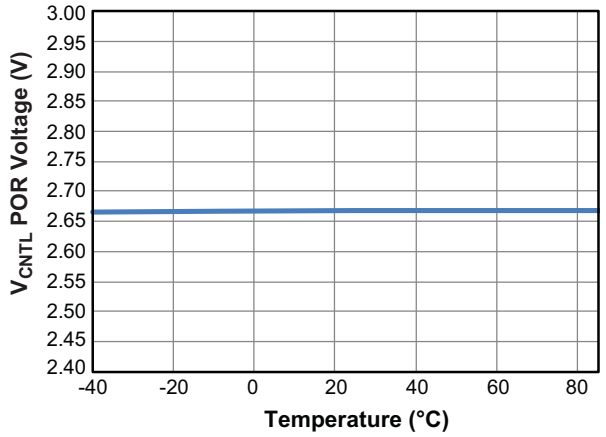

**$V_{CNTL}$ Standby Current vs. Temperature**




**Reference Voltage vs. Temperature**




**$V_{CNTL}$ POR Threshold Voltage vs. Temperature**



## Application Information

### Output Voltage Setting

The output voltage can be set by the output voltage divider. Typically, the adjustable range of the output voltage is from 1V to ($V_{IN}$ - $V_{drop}$). The output voltage is set by the equation below:

$$V_{OUT} = 0.8V \times \frac{R1 + R2}{R2}$$

### Supply Voltage (VCNTL)

Supply voltage is used to provide the power for the internal circuits. For the device to regulate, the voltage on this pin must be at least 1.5V greater than the output voltage, and no less than $V_{CNTL\_min}$. A 0.1µF or more ceramic capacitor close to the pin is required to filter the control voltage.

### Enable (EN)

The EN pin is used to turn off the regulator by pulling this pin below 0.8V. When the linear regulator is operated in the disable mode, the quiescent current can be limited below several ten micro-amp level.

### Input / Output Capacitor

A 10µF or more capacitances for the input side (VIN) is necessary. This not only decouples the noise from input side, but also keeps the input impedance as low as possible. In addition, a 22µF or more capacitances for the VIN above 4.5V is recommended for much lower input impedance.

A 10µF output capacitor is typically used with a 0.1µF ceramic capacitor for the output terminal (VOUT). Internal type-II compensation network allows lower ESR capacitors without stability problem.

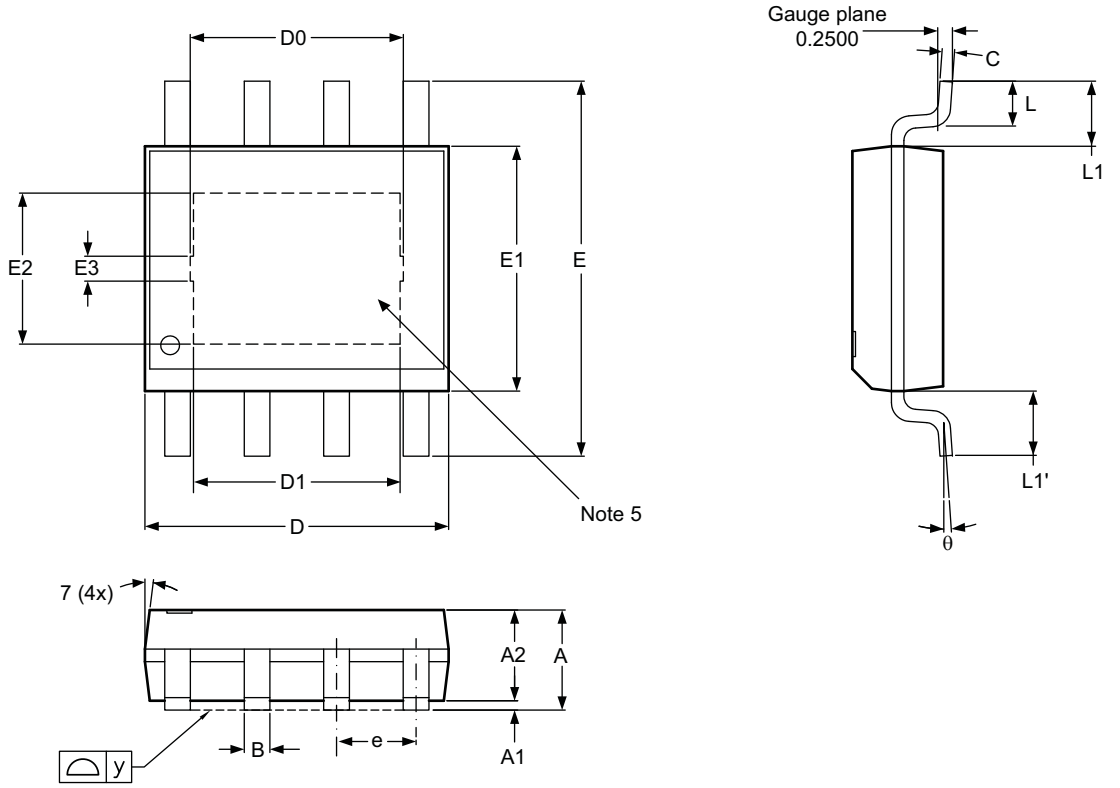
### Power OK (POK)

The POK pin is used to provide a logic signal to notice that the regulator works well. When the output voltage through the voltage divider is regulated above 90% of reference voltage, this pin will be as a high impedance status due to the open-drain output. An external pull-up resister is necessary to provide high-level signal. The sink capability of the POK pin is limited below 5mA. Typically, a 5.1kΩ resister for the 5V is recommended.

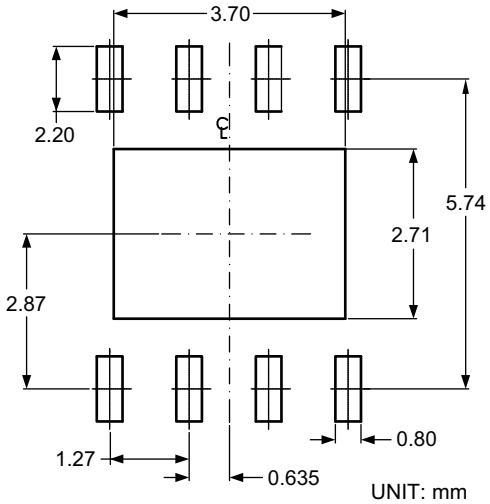
### Over Temperature Protection (OTP)

It is recommended that the junction temperature can be kept below the recommended operation condition 125 degree for maximum reliability. This power dissipation is conducted through the package into the ambient environment, and, in the process, the temperature of the die ($T_J$) rises above ambient.

## Package Dimensions, SO-8 EP1




### RECOMMENDED LAND PATTERN




**Dimensions in millimeters**

| Symbols | Min. | Nom. | Max. |
|---|---|---|---|
| A | 1.40 | 1.55 | 1.70 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.40 | 1.50 | 1.60 |
| B | 0.31 | 0.406 | 0.51 |
| C | 0.17 | — | 0.25 |
| D | 4.80 | 4.96 | 5.00 |
| D0 | 3.20 | 3.40 | 3.60 |
| D1 | 3.10 | 3.30 | 3.50 |
| E | 5.80 | 6.00 | 6.20 |
| e | — | 1.27 | — |
| E1 | 3.80 | 3.90 | 4.00 |
| E2 | 2.21 | 2.41 | 2.61 |
| E3 | 0.40 REF | | |
| L | 0.40 | 0.95 | 1.27 |
| y | — | — | 0.10 |
| θ | 0° | 3° | 8° |
| \| L1–L1' \| | — | 0.04 | 0.12 |
| L1 | 1.04 REF | | |

**Dimensions in inches**

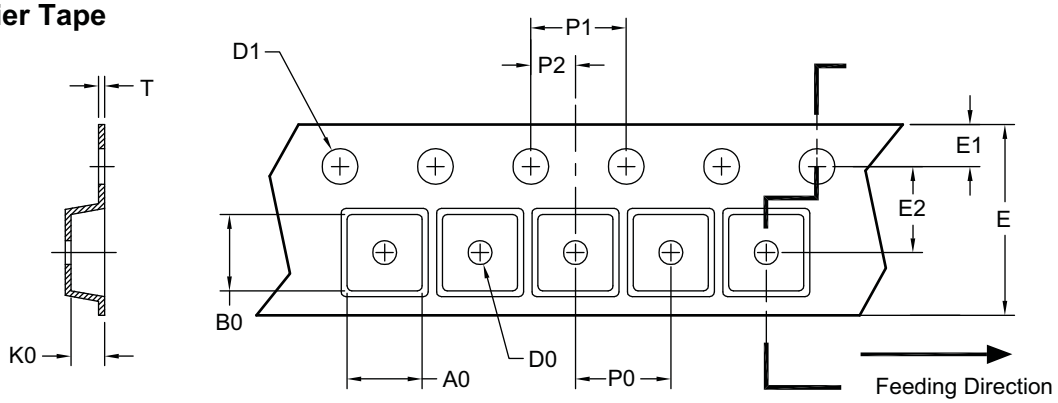
| Symbols | Min. | Nom. | Max. |
|---|---|---|---|
| A | 0.055 | 0.061 | 0.067 |
| A1 | 0.000 | 0.002 | 0.004 |
| A2 | 0.055 | 0.059 | 0.063 |
| B | 0.012 | 0.016 | 0.020 |
| C | 0.007 | — | 0.010 |
| D | 0.189 | 0.195 | 0.197 |
| D0 | 0.126 | 0.134 | 0.142 |
| D1 | 0.122 | 0.130 | 0.138 |
| E | 0.228 | 0.236 | 0.244 |
| e | — | 0.050 | — |
| E1 | 0.150 | 0.153 | 0.157 |
| E2 | 0.087 | 0.095 | 0.103 |
| E3 | 0.016 REF | | |
| L | 0.016 | 0.037 | 0.050 |
| y | — | — | 0.004 |
| θ | 0° | 3° | 8° |
| \| L1–L1' \| | — | 0.002 | 0.005 |
| L1 | 0.041 REF | | |

**Notes:**

1. Package body sizes exclude mold flash and gate burrs.
2. Dimension L is measured in gauge plane.
3. Tolerance 0.10mm unless otherwise specified.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.
5. Die pad exposure size is according to lead frame design.
6. Followed from JEDEC MS-012

## Tape and Reel Dimensions, SO-8 EP1

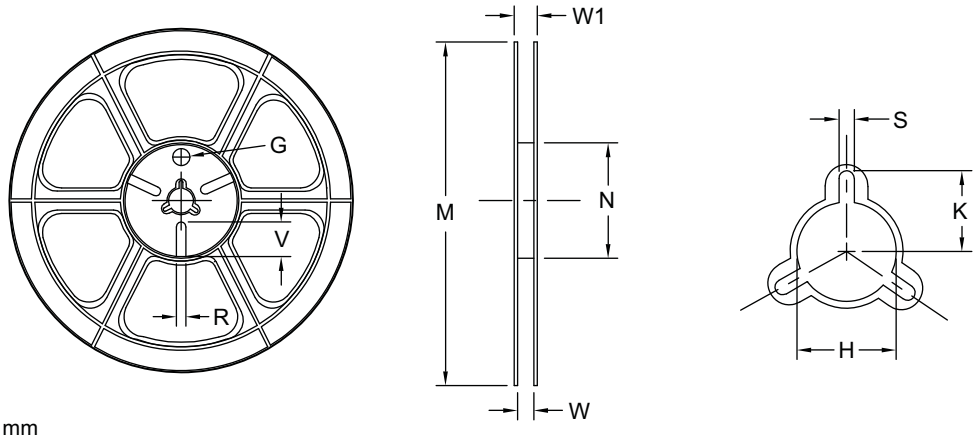
### Carrier Tape




UNIT: mm

| Package | A0 | B0 | K0 | D0 | D1 | E | E1 | E2 | P0 | P1 | P2 | T |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SO-8 (12mm) | 6.40 ±0.10 | 5.20 ±0.10 | 2.10 ±0.10 | 1.60 ±0.10 | 1.50 ±0.10 | 12.00 ±0.10 | 1.75 ±0.10 | 5.50 ±0.10 | 8.00 ±0.10 | 4.00 ±0.10 | 2.00 ±0.10 | 0.25 ±0.10 |

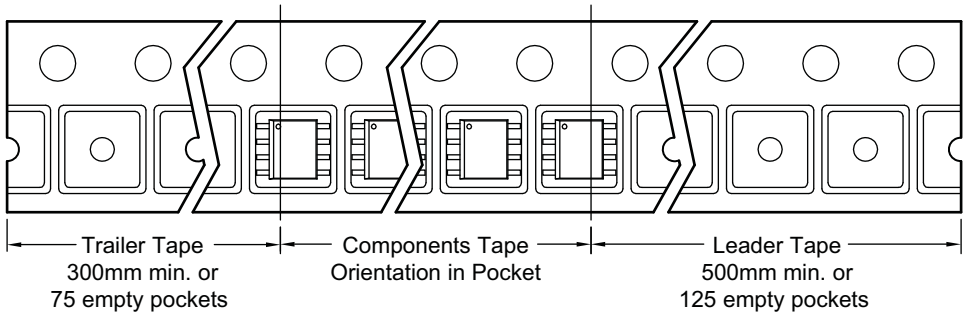
### Reel




UNIT: mm

| Tape Size | Reel Size | M | N | W | W1 | H | K | S | G | R | V |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 12mm | ø330 | ø330.00 ±0.50 | ø97.00 ±0.10 | 13.00 ±0.30 | 17.40 ±1.00 | ø13.00 +0.50/-0.20 | 10.60 | 2.00 ±0.50 | — | — | — |

### Leader/Trailer and Orientation



## Part Marking

**AOZ2002PI**
**(SO-8)**