

# 74F322

## Octal Serial/Parallel Register with Sign Extend

### General Description

The 74F322 is an 8-bit shift register with provision for either serial or parallel loading and with 3-STATE parallel outputs plus a bi-state serial output. Parallel data inputs and parallel outputs are multiplexed to minimize pin count. State changes are initiated by the rising edge of the clock. Four synchronous modes of operation are possible: hold (store), shift right with serial entry, shift right with sign extend and

parallel load. An asynchronous Master Reset ( $\overline{MR}$ ) input overrides clocked operation and clears the register.

### Features

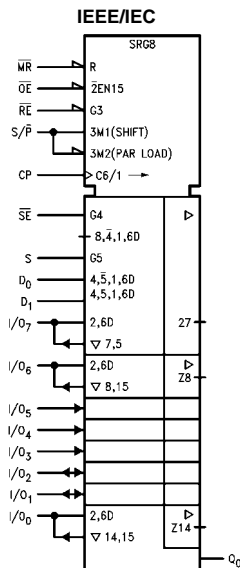
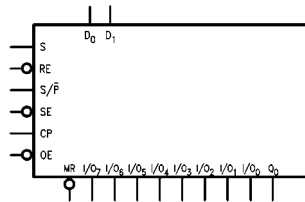
- Multiplexed parallel I/O ports
- Separate serial input and output
- Sign extend function
- 3-STATE outputs for bus applications

### Ordering Code:

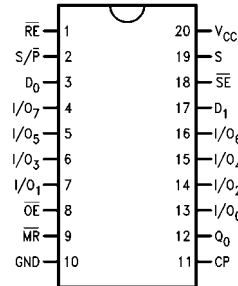
Order Number	Package Number	Package Description
74F322PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbols



### Connection Diagram



74F322 Octal Serial/Parallel Register with Sign Extend

## Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{RE}$	Register Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$S/\overline{P}$	Serial (HIGH) or Parallel (LOW) Mode Control Input	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{SE}$	Sign Extend Input (Active LOW)	1.0/3.0	20 $\mu$ A/-1.8 mA
S	Serial Data Select Input	1.0/2.0	20 $\mu$ A/-1.2 mA
$D_0, D_1$	Serial Data Inputs	1.0/1.0	20 $\mu$ A/-0.6 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$\overline{OE}$	3-STATE Output Enable Input (Active LOW)	1.0/1.0	20 $\mu$ A/-0.6 mA
$Q_0$	Bi-State Serial Output	50/33.3	-1 mA/-20 mA
$I/O_0$ - $I/O_7$	Multiplexed Parallel Data Inputs or 3-STATE Parallel Data Outputs	3.5/1.083 150/40 (33.3)	70 $\mu$ A/-0.65 mA -3 mA/24 mA (20 mA)

## Functional Description

The 74F322 contains eight D-type edge triggered flip-flops and the interstage gating required to perform right shift and the intrastage gating necessary for hold and synchronous parallel load operations. A LOW signal on  $\overline{RE}$  enables shifting or parallel loading, while a HIGH signal enables the hold mode. A HIGH signal on  $S/\overline{P}$  enables shift right, while a LOW signal disables the 3-STATE output buffers and enables parallel loading. In the shift right mode a HIGH sig-

nal on  $\overline{SE}$  enables serial entry from either  $D_0$  or  $D_1$ , as determined by the S input. A LOW signal on  $\overline{SE}$  enables shift right but  $Q_7$  reloads its contents, thus performing the sign extend function required for the 74F384 Twos Complement Multiplier. A HIGH signal on  $\overline{OE}$  disables the 3-STATE output buffers, regardless of the other control inputs. In this condition the shifting and loading operations can still be performed.

## Mode Select Table

Mode	Inputs							Outputs								$Q_0$
	$\overline{MR}$	$\overline{RE}$	$S/\overline{P}$	$\overline{SE}$	S	$\overline{OE}$ (Note 1)	CP	$I/O_7$	$I/O_6$	$I/O_5$	$I/O_4$	$I/O_3$	$I/O_2$	$I/O_1$	$I/O_0$	
Clear	L	X	X	X	X	L	X	L	L	L	L	L	L	L	L	L
	L	X	X	X	X	H	X	Z	Z	Z	Z	Z	Z	Z	Z	L
Parallel Load	H	L	L	X	X	X	$\curvearrowright$	$I_7$	$I_6$	$I_5$	$I_4$	$I_3$	$I_2$	$I_1$	$I_0$	$I_0$
Shift	H	L	H	H	L	L	$\curvearrowright$	$D_0$	$O_7$	$O_6$	$O_5$	$O_4$	$O_3$	$O_2$	$O_1$	$O_1$
Right	H	L	H	H	H	L	$\curvearrowright$	$D_1$	$O_7$	$O_6$	$O_5$	$O_4$	$O_3$	$O_2$	$O_1$	$O_1$
Sign Extend	H	L	H	L	X	L	$\curvearrowright$	$O_7$	$O_7$	$O_6$	$O_5$	$O_4$	$O_3$	$O_2$	$O_1$	$O_1$
Hold	H	H	X	X	X	L	$\curvearrowright$	NC	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level

L = LOW Voltage Level

Z = High Impedance Output State

$\curvearrowright$  = LOW-to-HIGH Transition

NC = No Change

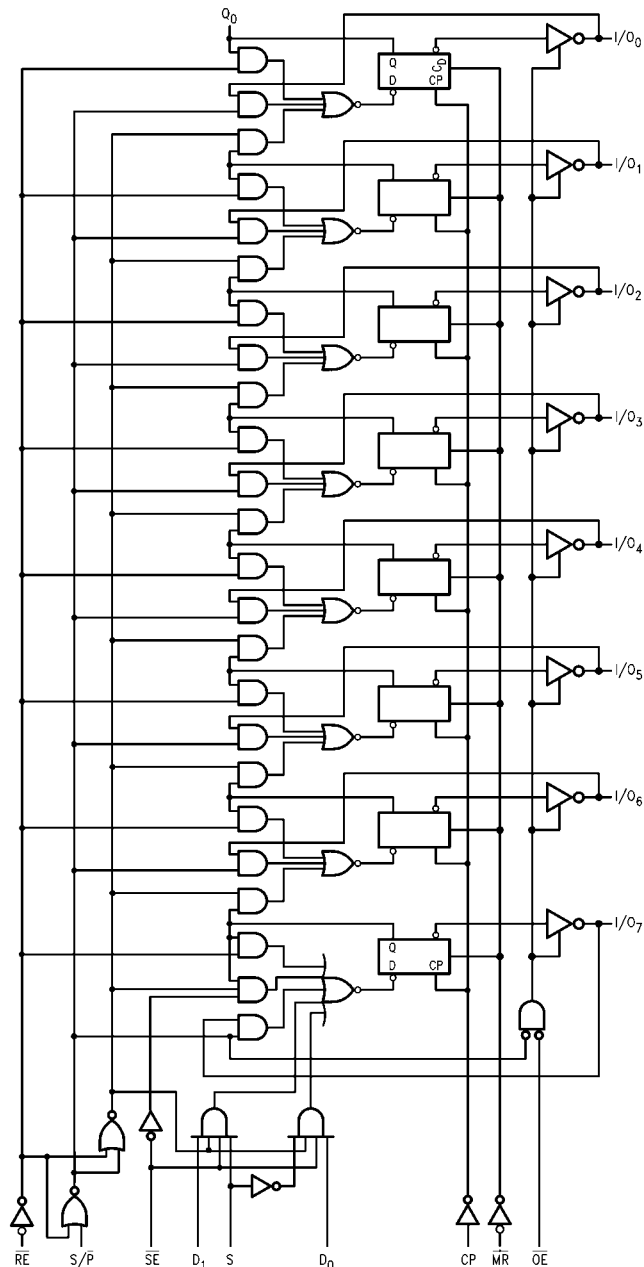
**Note:**  $I_7$ - $I_0$  = The level of the steady-state input at the respective I/O terminal is loaded into the flip-flop while the flip-flop outputs (except  $Q_0$ ) are isolated from the I/O terminal.

**Note:**  $D_0, D_1$  = The level of the steady-state inputs to the serial multiplexer input.

**Note:**  $O_7$ - $O_0$  = The level of the respective  $Q_n$  flip-flop prior to the last Clock LOW-to-HIGH transition.

**Note 1:** When the  $\overline{OE}$  input is HIGH all  $I/O_n$  terminals are at the high impedance state; sequential operation or clearing of the register is not affected.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 2)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 3)	-0.5V to +7.0V
Input Current (Note 3)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 2:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 3:** Either voltage limit or current limit is sufficient to protect inputs.

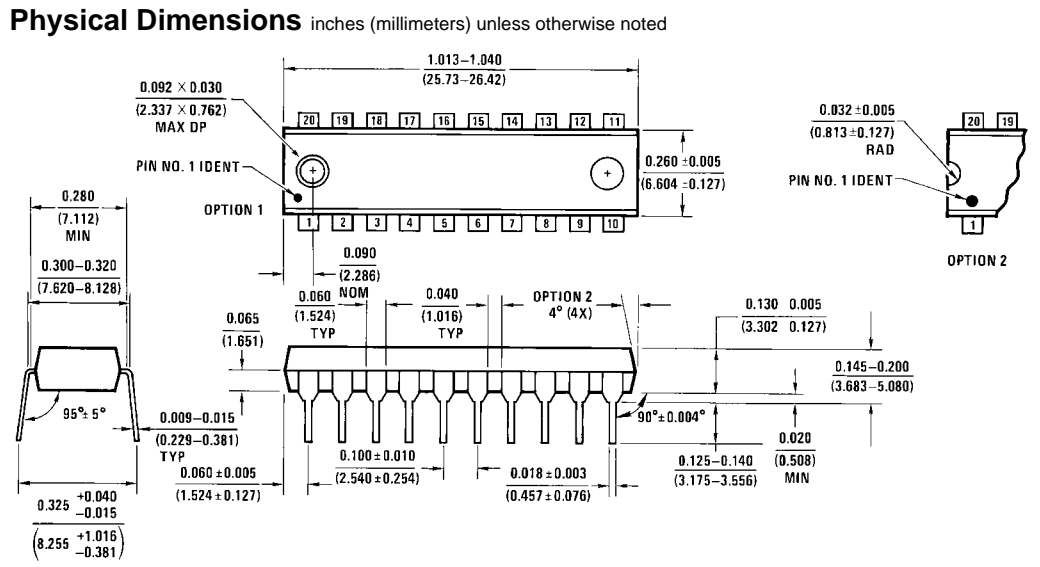
**DC Electrical Characteristics**

Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub> 5% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.4 2.7 2.7		V	Min	I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , I/O <sub>n</sub> ) I <sub>OH</sub> = -3 mA (I/O <sub>n</sub> ) I <sub>OH</sub> = -1 mA (Q <sub>0</sub> , I/O <sub>n</sub> ) I <sub>OH</sub> = -3 mA (I/O <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub> 10% V <sub>CC</sub>		0.5 0.5	V	Min	I <sub>OL</sub> = 20 mA (Q <sub>0</sub> ) I <sub>OL</sub> = 24 mA (I/O <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V (Non-I/O Inputs)
I <sub>BVIT</sub>	Input HIGH Current Breakdown Test (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (I/O <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6 -1.2 -1.8	mA	Max	V <sub>IN</sub> = 0.5V (RE, S/P, D <sub>n</sub> , CP, MR, OE) V <sub>IN</sub> = 0.5V (S) V <sub>IN</sub> = 0.5V (SE)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>I/O</sub> = 2.7V (I/O <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>I/O</sub> = 0.5V (I/O <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-60		-150	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CC</sub>	Power Supply Current		60	90	mA	Max	

AC Electrical Characteristics									
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $C_L = 50\text{ pF}$		$T_A = 0^\circ\text{C to } +75^\circ\text{C}$ $C_L = 50\text{ pF}$		Units
		Min	Typ	Max	Min	Max	Min	Max	
$f_{\text{MAX}}$	Maximum Clock Frequency	70	90		50		70		MHz
$t_{\text{PLH}}$	Propagation Delay	3.5	7.0	7.5	3.5	9.5	3.5	8.5	ns
$t_{\text{PHL}}$	CP to $I/O_n$	5.0	8.5	11.0	3.5	10.0	5.0	12.0	
$t_{\text{PLH}}$	Propagation Delay	3.5	7.0	9.0	3.5	11.0	3.5	10.0	ns
$t_{\text{PHL}}$	CP to $Q_0$	3.5	7.0	8.0	3.5	10.0	3.5	9.0	
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{MR}}$ to $I/O_n$	6.0	10.0	13.0	6.0	15.0	6.0	14.0	ns
$t_{\text{PHL}}$	Propagation Delay $\overline{\text{MR}}$ to $Q_0$	5.5	7.5	12.0	5.5	14.0	5.5	13.0	ns
$t_{\text{PZH}}$	Output Enable Time	3.0	6.5	9.0	3.0	12.5	3.0	10.0	ns
$t_{\text{PZL}}$	$\overline{\text{OE}}$ to $I/O_n$	4.0	8.5	11.0	4.0	14.5	4.0	12.0	
$t_{\text{PHZ}}$	Output Disable Time	2.0	4.5	6.0	2.0	8.0	2.0	7.0	ns
$t_{\text{PLZ}}$	$\overline{\text{OE}}$ to $I/O_n$	2.0	5.0	7.0	2.0	10.0	2.0	8.0	
$t_{\text{PZH}}$	Output Enable Time	4.5	8.0	10.5	4.5	13.5	4.5	11.5	ns
$t_{\text{PZL}}$	$S/\overline{\text{P}}$ to $I/O_n$	5.5	10.0	14.0	5.5	17.0	5.5	15.0	
$t_{\text{PHZ}}$	Output Disable Time	5.0	9.0	11.5	5.0	16.5	5.0	12.5	ns
$t_{\text{PLZ}}$	$S/\overline{\text{P}}$ to $I/O_n$	6.0	12.0	15.5	6.0	19.5	6.0	16.5	

AC Operating Requirements								
Symbol	Parameter	$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$		$T_A = 0^\circ\text{C to } +75^\circ\text{C}$		Units
		Min	Max	Min	Max	Min	Max	
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	6.0		14.0		7.0		ns
$t_{\text{S}}(\text{L})$	$\overline{\text{RE}}$ to CP	14.0		18.0		16.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	0		0		0		ns
$t_{\text{H}}(\text{L})$	$\overline{\text{RE}}$ to CP	0		0		0		
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	6.5		8.5		7.5		ns
$t_{\text{S}}(\text{L})$	$D_0, D_1$ or $I/O_n$ to CP	6.5		8.5		7.5		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	2.0		3.0		3.0		ns
$t_{\text{H}}(\text{L})$	$D_0, D_1$ or $I/O_n$ to CP	2.0		3.0		3.0		
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	7.0		9.0		8.0		ns
$t_{\text{S}}(\text{L})$	$\overline{\text{SE}}$ to CP	2.5		11.0		3.5		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	2.0		2.0		2.0		ns
$t_{\text{H}}(\text{L})$	$\overline{\text{SE}}$ to CP	0.0		1.0		0.0		
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	11.0		13.0		12.0		ns
$t_{\text{S}}(\text{L})$	$S/\overline{\text{P}}$ to CP	13.5		21.0		15.5		
$t_{\text{S}}(\text{H})$	Setup Time, HIGH or LOW	6.5		8.5		7.5		ns
$t_{\text{S}}(\text{L})$	S to CP	9.0		11.0		10.0		
$t_{\text{H}}(\text{H})$	Hold Time, HIGH or LOW	0		1.0		0		ns
$t_{\text{H}}(\text{L})$	S or $S/\overline{\text{P}}$ to CP	0		0		0		
$t_{\text{W}}(\text{H})$	CP Pulse Width, HIGH or LOW	7.0		8.0		7.0		ns
$t_{\text{W}}(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW	5.5		7.5		6.5		
$t_{\text{REC}}$	Recovery Time $\overline{\text{MR}}$ to CP	8.0		12.0		8.0		ns



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A**

N20A (REV G)

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