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# FDD86252

## N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 150 V, 27 A, 52 mΩ

### Features

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)}$  = 52 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 5\text{ A}$
- Max  $r_{DS(on)}$  = 72 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 4\text{ A}$
- 100% UIL tested
- RoHS Compliant

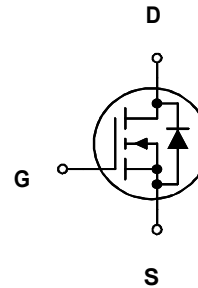
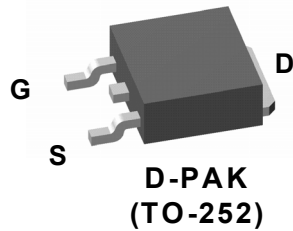


### General Description

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for the on-state resistance and yet maintain superior switching performance.

### Application

- DC - DC Conversion



### MOSFET Maximum Ratings $T_C = 25\text{ °C}$ unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	150	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous $T_C = 25\text{ °C}$	27	A
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	5	
	-Pulsed (Note 4)	30	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	72	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	89	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	3.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	40	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD86252	FDD86252	D-PAK(TO-252)	13 "	16 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		104		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 120\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-10		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 5\ \text{A}$		41	52	m $\Omega$
		$V_{GS} = 6\ \text{V}, I_D = 4\ \text{A}$		49	72	
		$V_{GS} = 10\ \text{V}, I_D = 5\ \text{A}, T_J = 125\text{ }^\circ\text{C}$		81	103	
$g_{FS}$	Forward Transconductance	$V_{DS} = 10\ \text{V}, I_D = 5\ \text{A}$		15		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 75\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		741	985	pF
$C_{oss}$	Output Capacitance			78	130	pF
$C_{rss}$	Reverse Transfer Capacitance			4.2	10	pF
$R_g$	Gate Resistance			0.4		$\Omega$

### Switching Characteristics

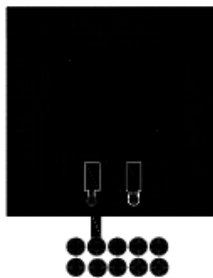
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 75\ \text{V}, I_D = 5\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		8.3	17	ns
$t_r$	Rise Time			1.8	10	ns
$t_{d(off)}$	Turn-Off Delay Time			14	25	ns
$t_f$	Fall Time			3	10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 10\ \text{V}$	$V_{DD} = 75\ \text{V},$ $I_D = 5\ \text{A}$	11.3	16	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\ \text{V to } 5\ \text{V}$		6.3	9	nC
$Q_{gs}$	Gate to Source Charge			3.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			2.6		nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source-Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 5\ \text{A}$ (Note 2)		0.80	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 2.6\ \text{A}$ (Note 2)		0.77	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 5\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		60	97	ns
$Q_{rr}$	Reverse Recovery Charge			72	115	nC

#### Notes:

- 1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta JA}$  is determined by the user's board design.



a)  $40\text{ }^\circ\text{C/W}$  when mounted on a  $1\ \text{in}^2$  pad of 2 oz copper



b)  $96\text{ }^\circ\text{C/W}$  when mounted on a minimum pad

2: Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3: Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\ \text{mH}$ ,  $I_{AS} = 12\ \text{A}$ ,  $V_{DD} = 135\ \text{V}$ ,  $V_{GS} = 10\ \text{V}$ .

4: Pulsed Drain current is tested at 300  $\mu\text{s}$  with 2% duty cycle. For repetitive pulses, the pulse width is limited by the maximum junction temperature.

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted

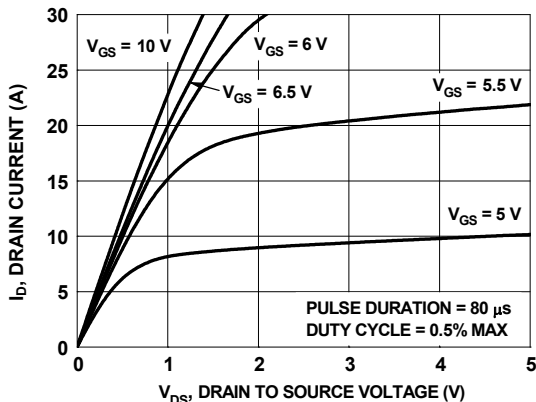


Figure 1. On-Region Characteristics

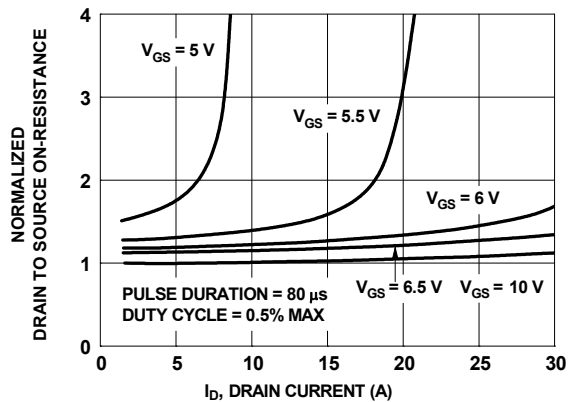


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

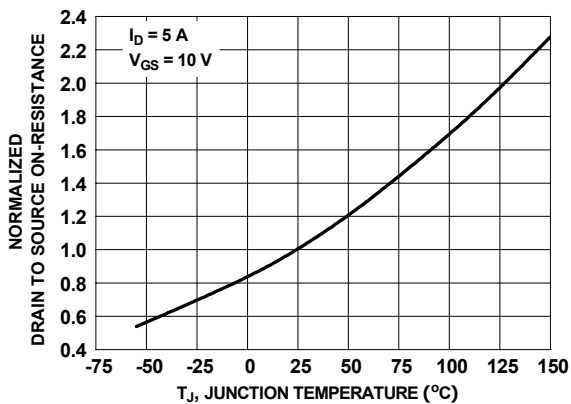


Figure 3. Normalized On-Resistance vs Junction Temperature

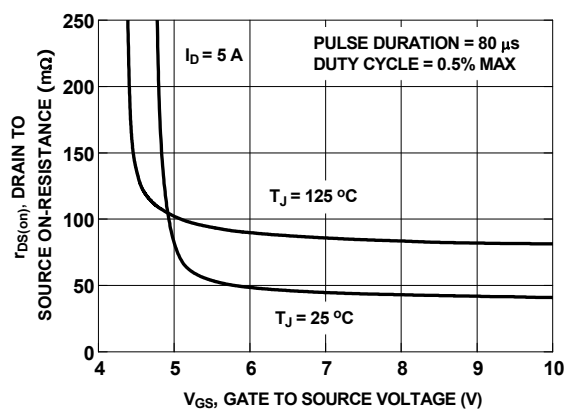


Figure 4. On-Resistance vs Gate to Source Voltage

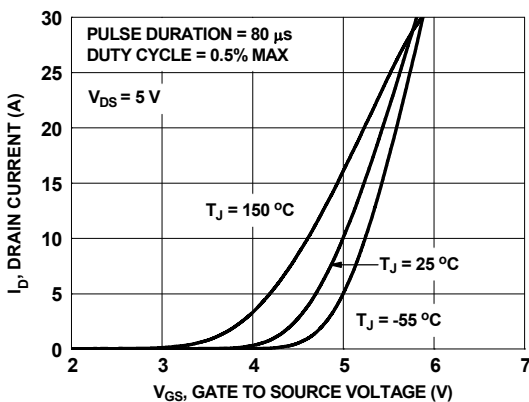


Figure 5. Transfer Characteristics

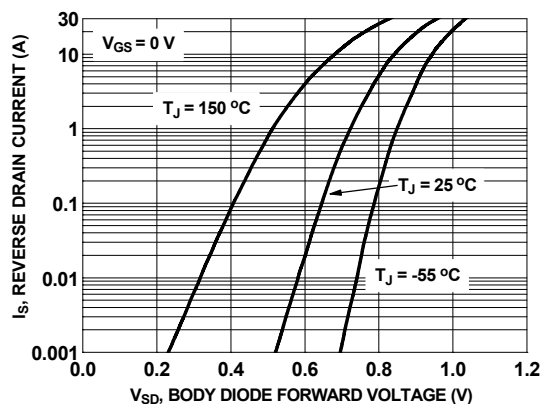
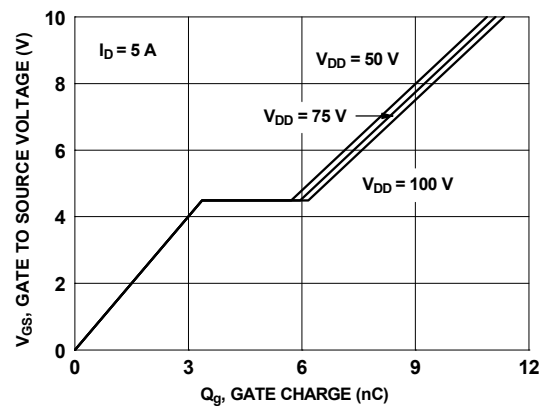
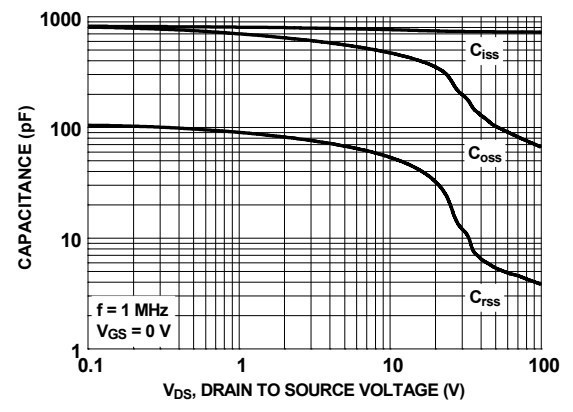


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

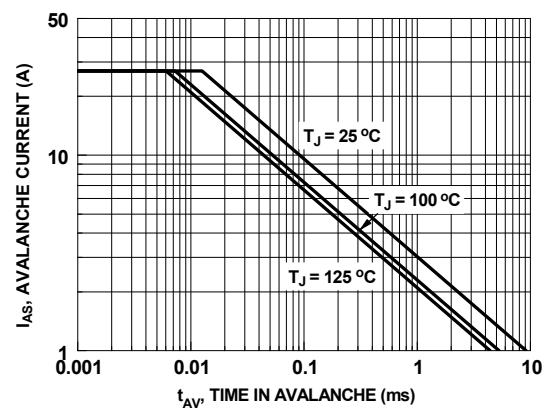
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



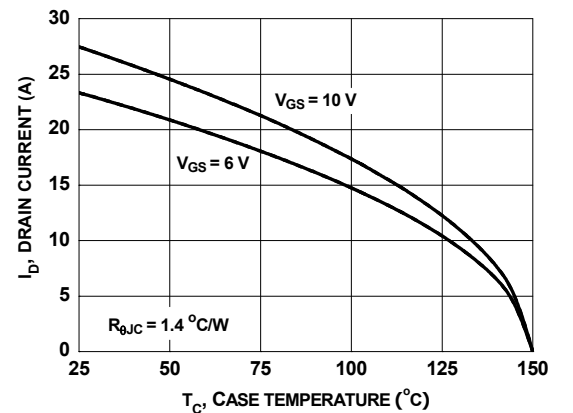
**Figure 7. Gate Charge Characteristics**



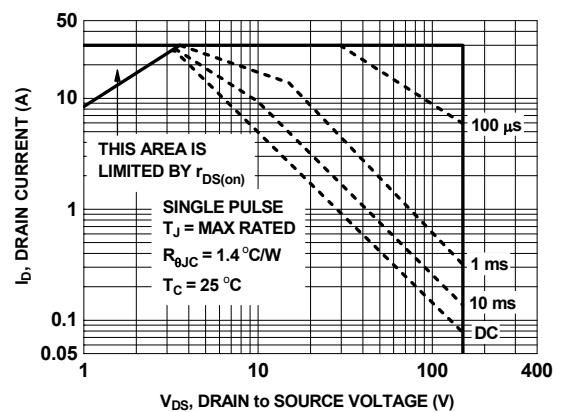
**Figure 8. Capacitance vs Drain to Source Voltage**



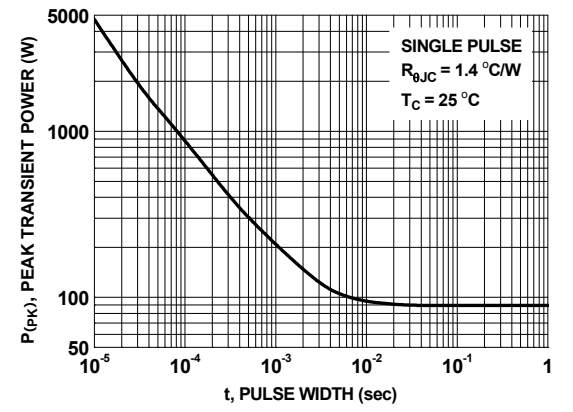
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Case Temperature**

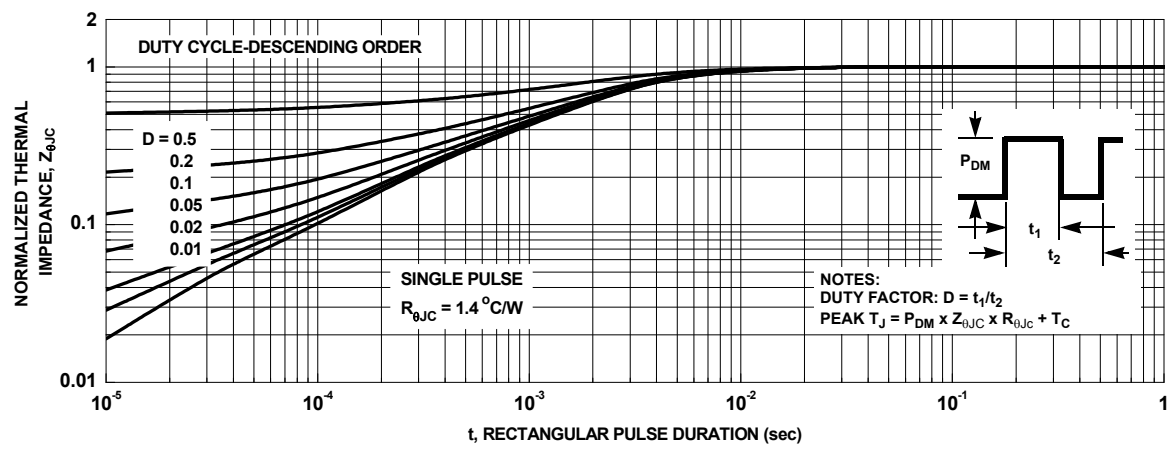


**Figure 11. Forward Bias Safe Operating Area**

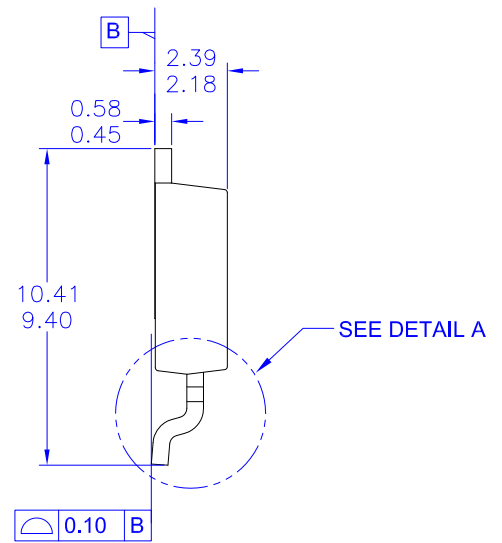


**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



**Figure 13. Junction-to-Case Transient Thermal Response Curve**



NOTES: UNLESS OTHERWISE SPECIFIED  
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

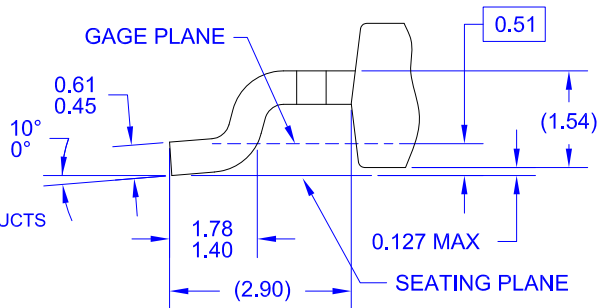
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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