PM6675A

High efficiency step-down controller with embedded 2A LDO regulator

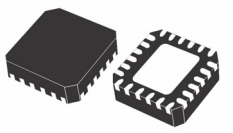
Target Specification

Features switching

- Switching section
  - 4.5V to 36V input voltage range
  - 0.6V, ±1% voltage reference
  - Selectable 1.5V fixed output voltage
  - Adjustable 0.6V to 3.3V output voltage
  - 1.237V ±1% reference voltage available
  - Very fast load transient response using constant-on-time control loop
  - No R_{SENSE} current sensing using low side MOSFETs' $R_{DS(ON)}$
  - Negative current limit
  - Latched OVP and UVP
  - Soft start internally fixed at 3ms
  - Selectable pulse skipping at light load
  - Selectable No-Audible (33KHz) pulse skip mode
  - Ceramic output capacitors supported
  - Output voltage ripple compensation
  - Output soft-end
- LDO regulator section
  - Adjustable 0.6V to 2.5V output voltage
  - Selectable ±1Apk or ±2Apk current limit
  - Dedicated power-good signal
  - Ceramic output capacitors supported
  - Output soft-end

Applications

- Industrial application on 24V
- Graphic cards
- Embedded computer systems



VFQFPN-24 4x4

Description

The PM6675A device consists of a single high efficiency step-down controller and an independent Low Drop-Out (LDO) linear regulator.

The Constant On-Time (COT) architecture assures fast transient response supporting both electrolytic and ceramic output capacitors. An embedded integrator control loop compensates the DC voltage error due to the output ripple.

Selectable low-consumption mode allows the highest efficiency over a wide range of load conditions. The low-noise mode sets the minimum switching frequency to 33kHz for audio-sensitive applications. The LDO linear regulator can sink and source up to 2Apk. Two fixed current limit (±1A- ±2A) can be chosen.

An active Soft-End is independently performed on both the switching and the linear regulators outputs when disabled.

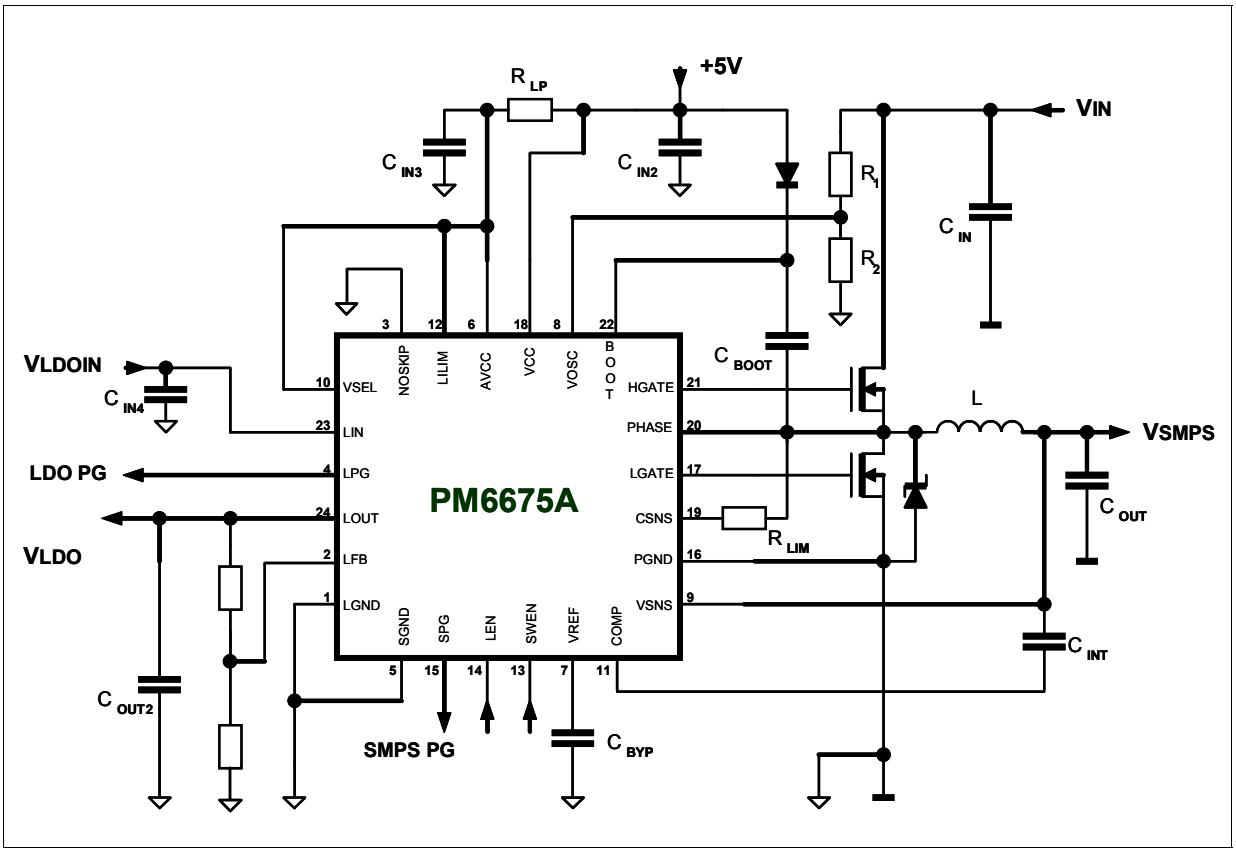
Order codes

Part number	Package	Packaging
PM6675A	VFQFPN-24 4x4 (Exposed Pad)	Tube

Contents

1 Typical application circuit

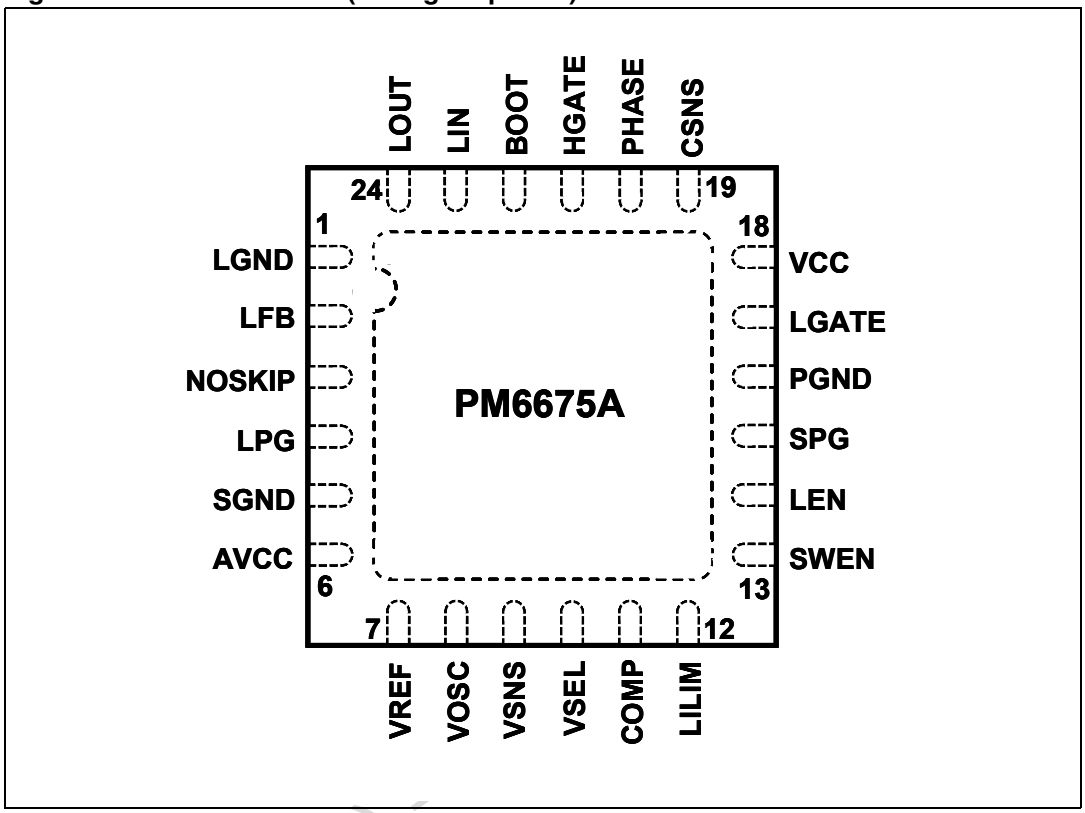
Figure 1. Application circuit



2 Pin settings

2.1 Connections

Figure 2. Pin connection (through top view)



2.2 Pin description

Table 1. Pin functions

N°	Pin	Function
1	LGND	LDO power ground. Connect to negative terminal of VTT output capacitor.
2	LFB	LDO remote sensing. Connect as close as possible to the load via a low noise PCB trace.
3	NOSKIP	Pulse-Skip/No-Audible Pulse-Skip Modes selector. See *Mode of Operation Selection* section for details.
4	LPG	LDO section Power-Good signal (open drain output). High when LDO output voltage is within ±10% of nominal value.
5	SGND	Ground Reference for analog circuitry, control logic and VTTREF buffer. Connect together with the thermal pad and VTTGND to a low impedance ground plane. See the *Application Note* for details.
6	AVCC	+5V supply for internal logic. Connect to +5V rail through a simple RC filtering network.
7	VREF	High accuracy output voltage reference (1.237V) for multilevel pins setting. It can deliver up to 50uA. Connect a 100nF capacitor between VREF and SGND in order to enhance noise rejection.
8	VOSC	Frequency Selection. Connect to the central tap of a resistor divider to set the desired switching frequency. The pin cannot be left floating. See *Device Description* section for details.
9	VSNS	Switching section output remote sensing and discharge path during output Soft-End. Connect as close as possible to the load via a low noise PCB trace.
10	VSEL	Fixed output selector and feedback input for the switching controller. If VSEL pin voltage is higher than 4V, the fixed 1.5V output is selected. If VSEL pin voltage is lower than 4V, it is used as negative input of the error amplifier. See *Mode of Operation Selection* section for details.
11	COMP	DC voltage error compensation pin for input the switching section. Refer to *Mode of Operation Selection* section for more details.
12	LILIM	Current limit selector for the LDO. Connect to SGND for ±1A current limit or to +5V for ±2A current limit.
13	SWEN	Switching Controller Enable. When tied to ground, the switching output is turned off and a Soft-End is performed.
14	LEN	Linear Regulator Enable. When tied to ground, the LDO output is turned off and a Soft-End is performed.
15	SPG	Switching Section Power-Good signal (open drain output). High when the switching regulator output voltage is within ±10% of nominal value.
16	PGND	Power ground for the switching section.
17	LGATE	Low-side gate driver output.
18	VCC	+5V low-side gate driver supply. Bypass with a 100nF capacitor to PGND.

Table 1. Pin functions (continued)

N°	Pin	Function
19	CSNS	Current sense input for the switching section. This pin must be connected through a resistor to the drain of the synchronous rectifier (RDSon sensing) or to the source of the synchronous rectifier (R_{SENSE} sensing) to set the current limit threshold.
20	PHASE	Switch node connection and return path for the high side gate driver.
21	HGATE	High-Side Gate Driver Output
22	BOOT	Bootstrap capacitor connection. Input for the supply voltage of the high-side gate driver.
23	LIN	Linear Regulator Input. Bypass to LGND by a 10µF ceramic capacitor for noise rejection enhancement.
24	LOUT	LDO linear regulator output. Bypass with a 20µF (2x10µF MLCC) filter capacitor.

3 Electrical data

3.1 Maximum rating

Table 2. Absolute maximum ratings (1)

Symbol	Parameter	Value	Unit
V_{AVCC}	AVCC to SGND	-0.3 to 6	V
V_{VCC}	VCC to SGND	-0.3 to 6	
	PGND, LGND to SGND	-0.3 to 0.3	
	HGATE and BOOT to PHASE	-0.3 to 6	
	HGATE and BOOT to PGND	-0.3 to 44	
V_{PHASE}	PHASE to SGND	-0.3 to 38	
	LGATE to PGND	-0.3 to V_{VCC} +0.3	
	CSNS, SPG, LEN, SWEN, LILIM, COMP, VSEL, VSNS, VOSC, VREF, NOSKIP to SGND	-0.3 to V_{AVCC} + 0.3	
	LPG,VREF, LOUT, LFB to SGND	-0.3 to V_{AVCC} + 0.3	
	LIN, LOUT, LPG, LIN to LGND	-0.3 to V_{AVCC} + 0.3	
P_{TOT}	Power dissipation @T_A = 25°C	2.3	W

1. Free air operating conditions unless otherwise specified. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction to ambient	42	°C/W
T_{STG}	Storage temperature range	-40 to 150	°C
T_A	Operating ambient temperature range	-40 to 85	°C
T_J	Junction operating temperature range	-25 to 125	°C

4 Electrical characteristics

T_A = 0°C to 85°C , VCC = AVCC = +5V, LIN = 1.5V and LOUT= 0.9V if not otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test condition		Min.	Typ.	Max.	Unit
Supply section							
V_{IN}	Input voltage range			4.5		36	V
V_{AVCC}	IC supply voltage			4.5		5.5	
V_{VCC}	IC supply voltage			4.5		5.5	
I_{IN}	Operating current (Switching + LDO)	SWEN, LEN, VSEL and NOSKIP connected to AVCC, No load on LOUT output.				2	mA
I_{SW}	Operating current (Switching)	SWEN, VSEL and NOSKIP connected to AVCC, LEN connected to SGND.				1	
I_{SHDN}	Shutdown operating current	SWEN and LEN tied to SGND.				10	µA
UVLO	AVCC Under Voltage Lockout upper threshold			4.0	4.1	4.2	V
	AVCC Under Voltage Lockout upper threshold			3.8	3.9	4.0	
	UVLO hysteresis			50			mV
ON-time (SMPS)							
t_{ON}	On-time duration	VSEL and NOSKIP high, V_{VSNS} = 2V	VOSC = 300mV	650	750	850	ns
			VOSC = 500mV	390	450	510	
OFF-time (SMPS)							
t_{OFFMIN}	Minimum Off-Time				300	350	ns
Voltage reference							
	Voltage accuracy	4.5V< V_{IN} < 25V		1.224	1.237	1.249	V
	Load regulation	-50µA< I_{VREF} < 50µA		-4		4	mV
	Undervoltage Lockout Fault Threshold				800		
SMPS output							
V_{OUT}	SMPS fixed output voltage (1)	VSEL connected to AVCC, NOSKIP tied to SGND, No Load			1.5		V
	Output voltage accuracy (1)			-2		2	%

1. Guaranteed by design. Not production tested.

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Current limit and zero crossing comparator						
I_{CSNS}	CSNS input bias current		90	100	110	µA
	Comparator offset		-5		5	mV
	Positive current limit threshold	V_{PGND} - V_{CSNS}	-115	-100	-85	
	Fixed negative current limit threshold		-130	-110	-90	
$V_{ZC,OFFS}$	Zero crossing comparatot offset		-10	-5	0	
High and low side gate drivers						
	HGATE driver on-resistance	HGATE high state (pullup)		2.0	3	Ω
		HGATE low state (pulldown)		1.8	2.7	
	LGATE driver on-resistance	LGATE high state(pullup)		1.4	2.1	
		LGATE low state (pulldown)		0.6	0.9	
UVP/OVP protections and PGOOD signals						
OVP	Over voltage threshold		112	115	118	%
UVP	Under voltage threshold		63	70	73	
PGOOD	SMPS upper threshold		107	110	113	
	SMPS lower threshold		87	90	93	
	LDO upper threshold		107	110	113	
	LDO lower threshold		87	90	93	
$I_{PG,LEAK}$	SPG and LPG leakeage current[1]	SPG and LPG forced to 5.5V			1	µA
$V_{PG,LOW}$	SPG and LPG low level voltage	$I_{LPG,SINK}$ = $I_{SPG,SINK}$ = 4mA		150	250	mV
Soft start section (SMPS)						
	Soft-start ramp time (4 steps current limit)		2	3	4	ms
	Soft-start initial current limit		22.5	25	27.5	µA
	Soft-start current limit step		22.5	25	27.5	
Soft end section						
	Switching section discharge resistance			25		Ω
	LDO section discharge resistance			25		
LDO section						
V_{LREF}	LDO reference voltage		0.594	0.6	0.606	V
V_{DROP}	LDO drop-out voltage	V_{LOUT} = 0.9V, I_{LOUT} =1A, -10% output drop		0.25		

Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
	LDO Internal high-side MOSFET $R_{DS(on)}$	I_{LOUT} = 1A, AVCC = 5V		0.2	0.23	Ω
$I_{LDO,CL}$	LDO source current limit	V_{LFB} < 1.10* V_{LREF} , LILIM = 5V	2	2.1	2.2	A
		V_{LFB} < 1.10* V_{LREF}, LILIM = 0V	1	1.1	1.2	
	LDO sink current limit	0.90* V_{LREF} < V_{LFB} < 1.10* V_{LREF}, LILIM = 5V	-2.2	-2.1	-2	
		0.90* V_{LREF} < V_{LFB} < 1.10* V_{LREF}, LILIM = 0V	-1.2	-1.1	-1	
		V_{LFB} > 1.10* V_{LREF}, LILIM = 5V	-1.2	-1.1	-1	
		V_{LFB} > 1.10* V_{LREF}, LILIM = 0V	-0.6	-0.55	-0.6	
$I_{LIN,BIAS}$	LDO input bias current, On	LEN connected to AVCC, no load		1	10	µA
	LDO input bias current, Off	LEN = 0V, no load			1	
$I_{LFB,BIAS}$	LFB input bias current	LEN connected to AVCC V_{LFB} = 0.6V	-1		1	
$I_{LFB,LEAK}$	LFB leakage current	LEN = 0V, V_{LFB} = 0.6V	-1		1	
Power management section						
$V_{VTHVSEL}$	VSEL pin thresholds	Fixed mode	4.3			V
		Adjustable mode			3.7	
$V_{VTHNOSKIP}$	NOSKIP pin thresholds (1)	Forced-PWM Mode	4.2			
		No-Audible Mode	1.0		3.5	
		Pulse-Skip Mode			0.5	
$V_{VTHLILIM}$	LILIM pin thresholds (1)	±2A LDO Current Limit	2.4			
		±1A LDO Current Limit			0.8	
$I_{IN,LEAK}$	Logic input leakage current (1)	LEN, SWEN and LILIM=5V			1	µA
$I_{IN3,LEAK}$	Multilevel input leakage current (1)	VSEL and NOSKIP=5V			1	
$I_{OSC,LEAK}$	VOSC pin leakage current (1)	VOSC=1V			1	
Thermal shutdown						
T_{SHDN}	Shutdown temperature (1)				150	°C

1. Guaranteed by design. Not production tested.

5 Block diagram

Figure 3. Functional and block diagram

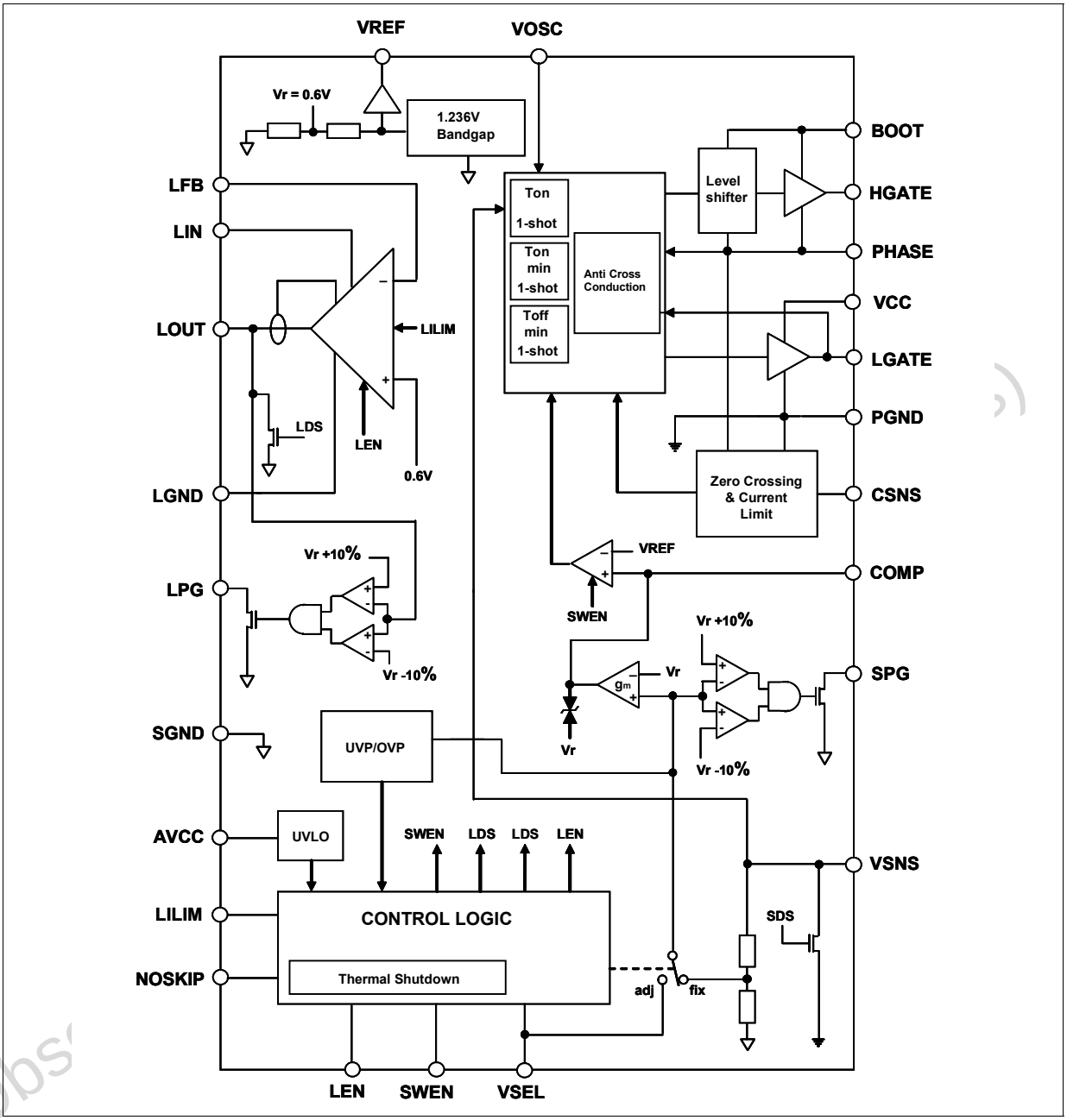


Table 6. Legend

SWEN	Switching controller enable
LEN	LDO regulator enable
LDS	LDO output discharge enable
SDS	Switching output discharge enable
LILIM	LDO regulator current limit

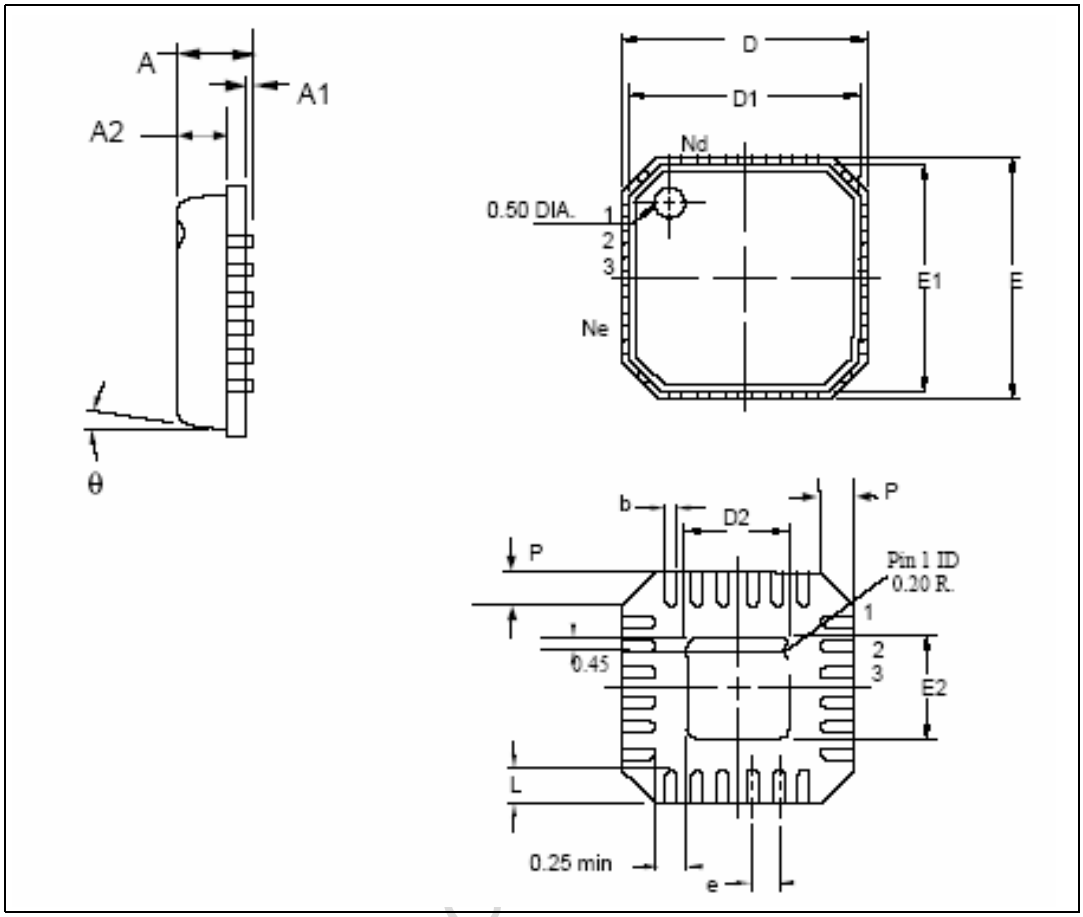
6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Table 7. VFQFPN-24 4mm x 4mm mechanical data

Dim.	mm.		
	Typ	Min.	Max.
A		0.80	1.00
A1	0.00	0.05	0.05
A2	0.65		0.80
D	4.00		
D1	3.75		
E	4.00		
E1	3.75		
θ			12°
P	0.42	0.24	0.60
e	0.50		
N	24.00		
Nd	6.00		
Ne	6.00		
L	0.40	0.30	0.50
b		0.18	0.30
D2	2.10	1.95	2.25
E2	2.10	1.95	2.25

Figure 4. Package dimensions



7 Revision history

Table 8. Revision history

Date	Revision	Changes
11-Oct-2006	1	Initial release.

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